Automatic Layout Synthesis of Transistors Networks for FDSOI

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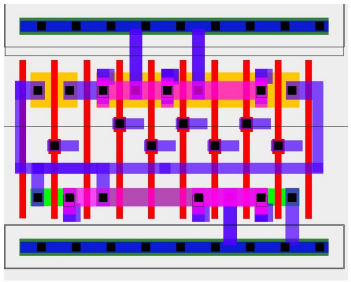
Motivation

It was developed a method and a tool for the automatic layout generation of transistors networks. The tool input is a netlist of a CMOS circuits. The tool is able to automatic generate the layout in a Fully Depleted Silicon on Insulator (FDSOI) technology at 28nm.



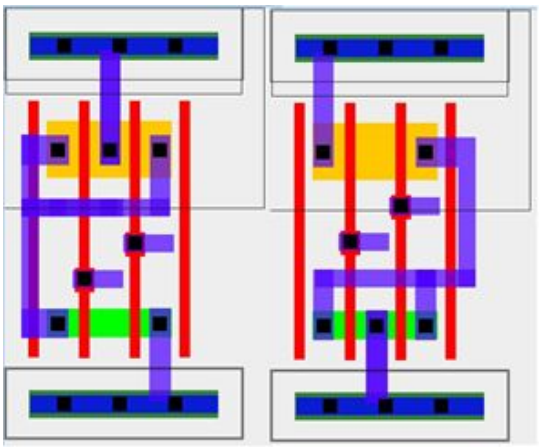
NOT(A.B.C.(D+E)+(F+G))

Methodology

INPUT: Transistor network netlist using a HSPICE format.

Placement of Transistors: Convolutions are applied in adjacency matrices generated for the PMOS network and the NMOS network, creating a third matrix, responsible for getting the Eulerian Path.

Routing: The input and output of the transistors are mapped, and connections are implemented. When two metal rectangles are on the same layer with divergent signals intersecting each other, one of them is moved to an upper layer



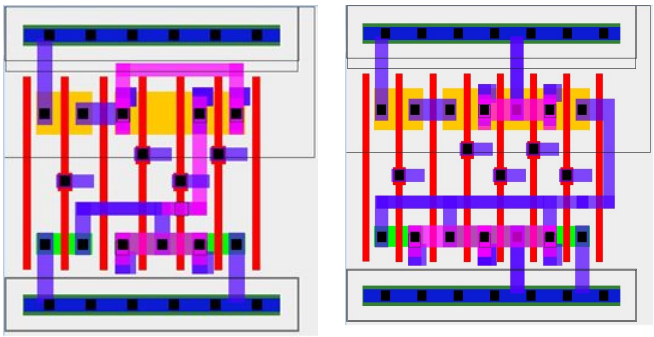
NAND2 NOR2

Results

The tool generate, as output, a list of rectangles translated to SKILL code. Tests were taken on an i3-5005U with 4GB ram. Table 1 shows, for each cell, the running time (in seconds) to generate its respective layout.

Logic Gate	Transistors	Time (s)
NAND2	4	4
NOR2	4	4
$\overline{(A+B).C}$	6	6
$\overline{(A.B+C.D).(E+F)}$	12	6
$\overline{A.B.C.(D+E)+(F+G)}$	14	6
$\overline{(A.B+C).D+(E.F+G.H).I}$	18	6
$\overline{(A.B+C.D)(E.F+G).(H.I+J.K)}$	22	8

Table 1: Generated Cells and its generation time



NOT(A+((B+C)D) NOT((A+B)C+(A+B)D+E)

Future Works

The next step is to define a convolutional neural network to optimize the routing and to adapt the tool to work with other technologies as FinFET 15nm and 7nm.