Contributions to OpenROAD from Abroad: Experiences and Learnings

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Introduction

We present:

How to become a contributor to the OpenROAD project (desired **skills**, differences from **academic research**)

The tools developed by us in the OpenROAD project (lessons learned from developing tools for **real** production ICs)

Challenges experienced and **best practices** adopted when working in a large project from abroad)

Becoming a contributor

Not research as usual

Build to last → Code quality and unit tests

Deliverables-driven

Recruiting

VLSI skills "vs" programming skills

Senior project members work together with undergrad CS and ECE students → *New EDA talents!*

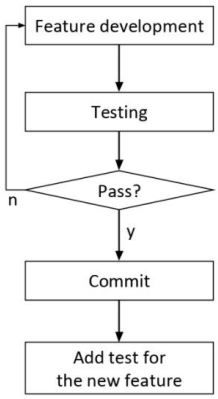
Logistics

UCSD visiting student status

Access to servers and enablements

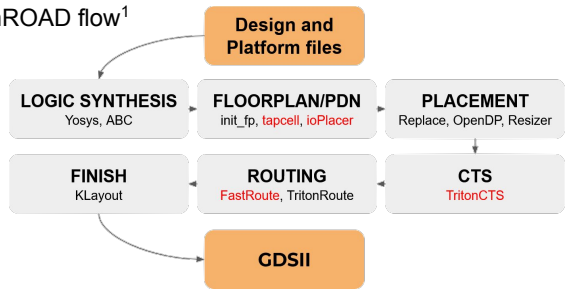
Internet connection

Language barrier



Our contributions

OpenROAD flow[1]



The tools highlighted in red are developed and maintained by the Brazilian team

Tools developed entirely for the project

Tapcell[2]

Straightforward task → lack of academic / open-source code

Support for 130nm down to 14nm

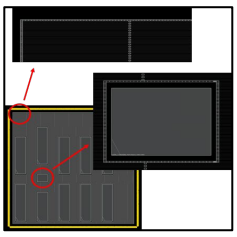
Logic developed by an experienced PD methodologist

ioPlacer[3]

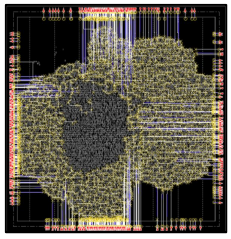
Neglected subject in VLSI CAD literature

Need to find I/O pin locations in block-level design

Fast and scalable Hungarian matching with divide-and-conquer



Tapcell insertion



I/O pin placement

Research code adapted for the OpenROAD flow

TritonCTS[4]

Adapted from the academic code GenHTree[5]

First open-source release removed all commercial tool dependencies, being a mix of C++ code and Tcl scripts → algorithm not scalable / code not extensible

Implementation of a second version, written from scratch in C++ → simple H-Tree code, integration with the project's STA tool, with support for clock gate cells, multiple clocks, generated clocks

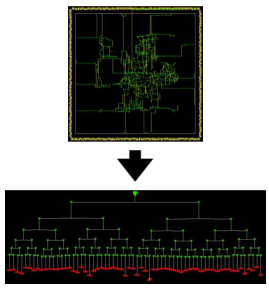
FastRoute[6]

Original code by Pan et al.[7] for a VLSI CAD contest

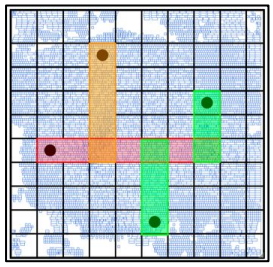
Overcoming code limitations: hard-coded max number of pins, layer direction, grid size, pin layers

Integration with detailed router: output in the guides file format

New features: technology tuning, antenna repair, parasitic estimation



Clock tree levels



Route guides example

Extreme partitioning

Integration of three partitioning tools: MLPart, Chaco and GPMetis under a single Tcl API

Allow user to generate many cluster solutions, with an evaluation API to find the best solution

The OpenROAD Experience

Working environment

Not research, not a company

Working with different universities and cultures!

Brazilian team unique characteristic: undergrad students

Valuable experience to future carrier

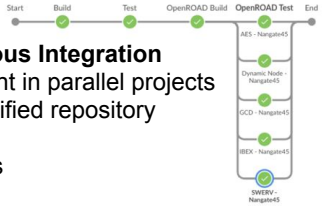
Working with industry veterans

Team organization and task management

Team is geographically spread → time zones impose a difficulty

Kanban-based project with Jira

"Task"-driven organization



Unified repository and Continuous Integration

Tools are in constant improvement in parallel projects

Integration of the tools into an unified repository

"Stable branch" for users

Per-tool unit tests and flow tests

References

[1] https://github.com/The-OpenROAD-Project/OpenROAD-flow-scripts
[2] https://github.com/The-OpenROAD-Project/OpenROAD/tree/master/src/tapcell
[3] V. Bandeira, M. Fogaça, E. Monteiro, I. Oliveira, M. Woo and R. Reis,"Fast and Scalable I/O Pin Assignment with Divide-and-Conquer andHungarian Matching",Proc. NEWCAS, 2020, pp. 1–4.
[4] https://github.com/The-OpenROAD-Project/OpenROAD/tree/master/src/TritonCTS
[5] K. Han, A. B. Kahng and J. Li, "Optimal Generalized H-Tree Topologyand Buffering for High-Performance and Low-Power Clock Distribu-tion",IEEE TCAD, 2020, pp. 478–491.
[6] https://github.com/The-OpenROAD-Project/OpenROAD/tree/master/src/FastRoute
[7] M. Pan, Y. Xu, Y. Zhang and C. Chu, "FastRoute: An Efficient andHigh-Quality Global Router",ACM VLSI Design, 2012, pp. 14:1–14:1.

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