Digital Integrated Circuits
A Design Perspective

Semiconductor Memories

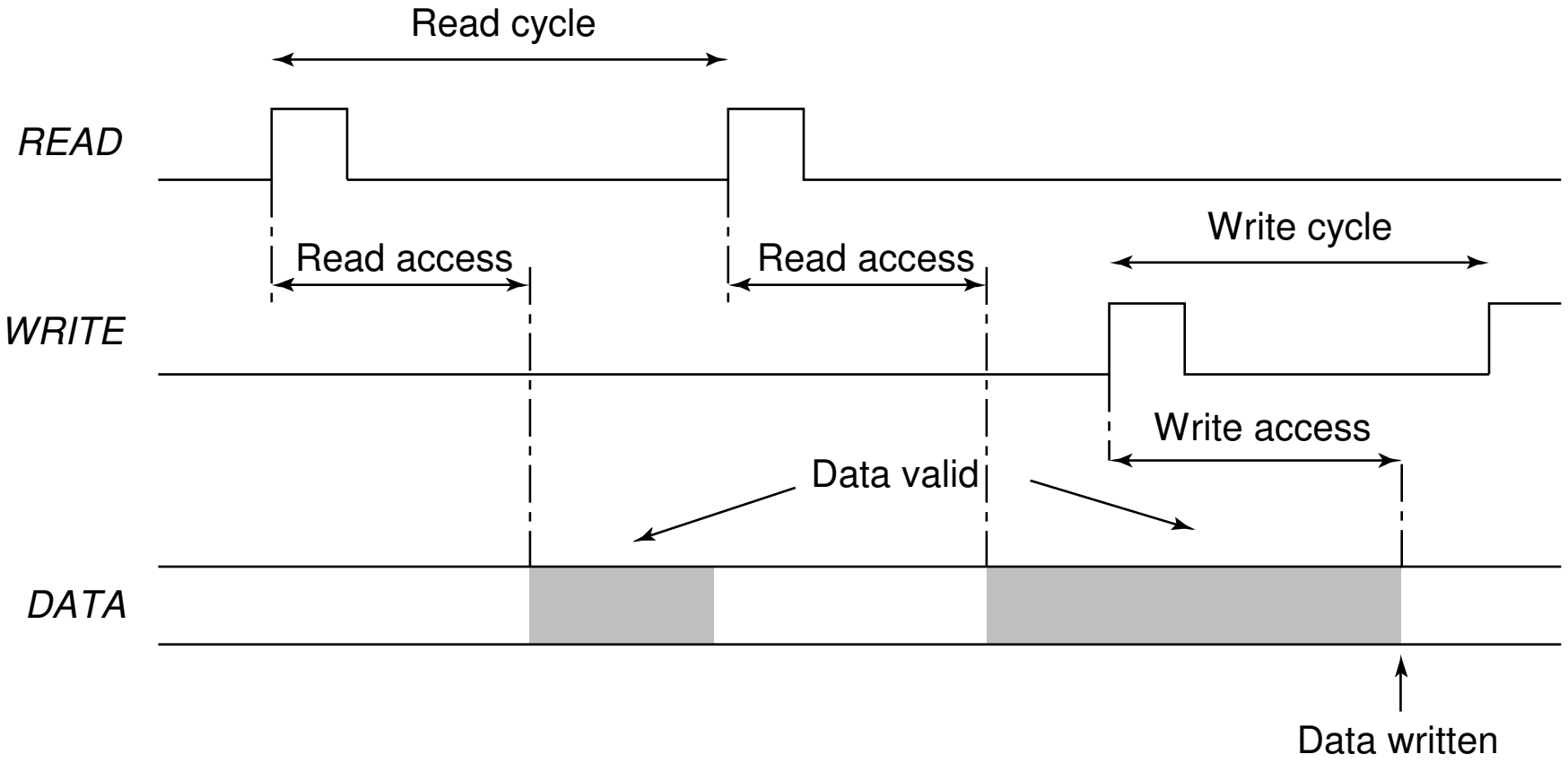
Reference: Digital Integrated Circuits, 2nd edition, Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic

Disclaimer: slides adapted for INE5442/EEL7312 by José L. Güntzel from the book´s companion slides made available by the authors.

Lecture Summary

- Memory Classification
- Memory Architectures
- The Memory Core (ROM Memories)

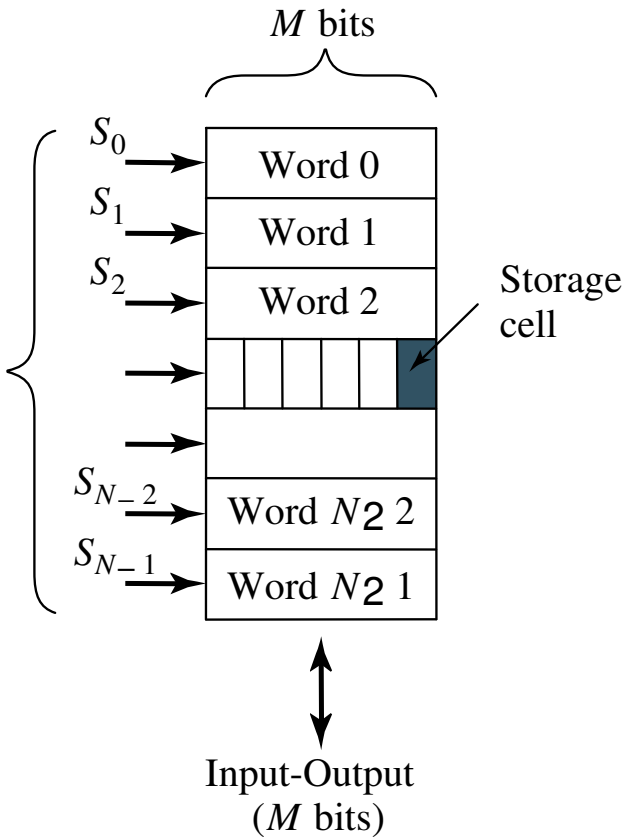
Memory Timing: Definitions

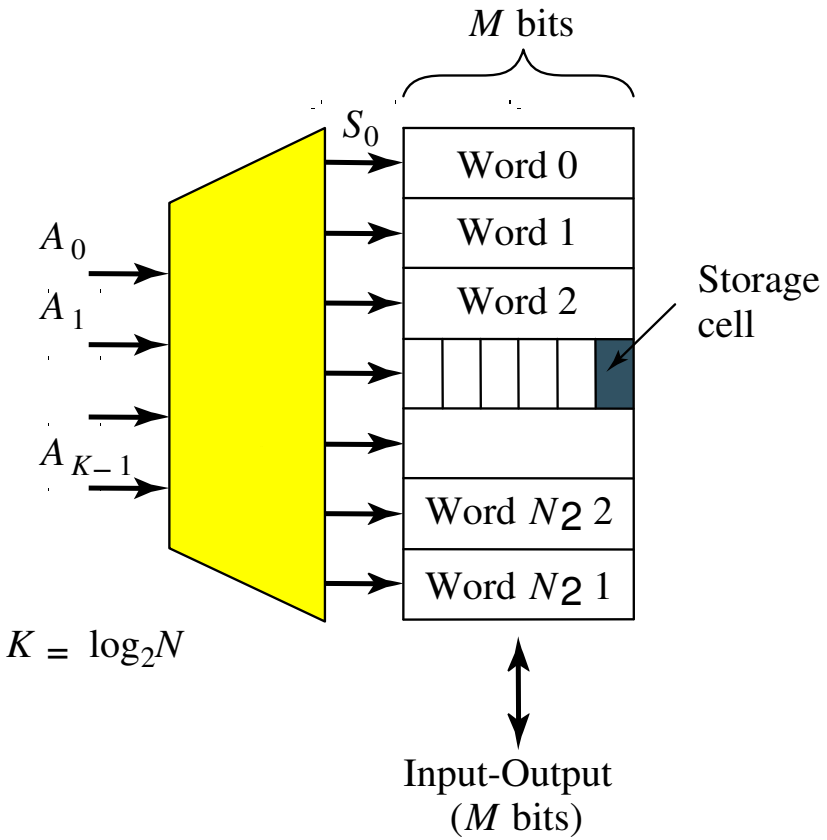


Semiconductor Memory Classification

Read-Write Memory		Non-Volatile Read-Write Memory	Read-Only Memory
Random Access	**Non-Random Access**	EPROM E^2PROM FLASH	Mask-Programmed Programmable (PROM)
SRAM DRAM	FIFO LIFO Shift Register CAM		

Memory Architecture: Decoders





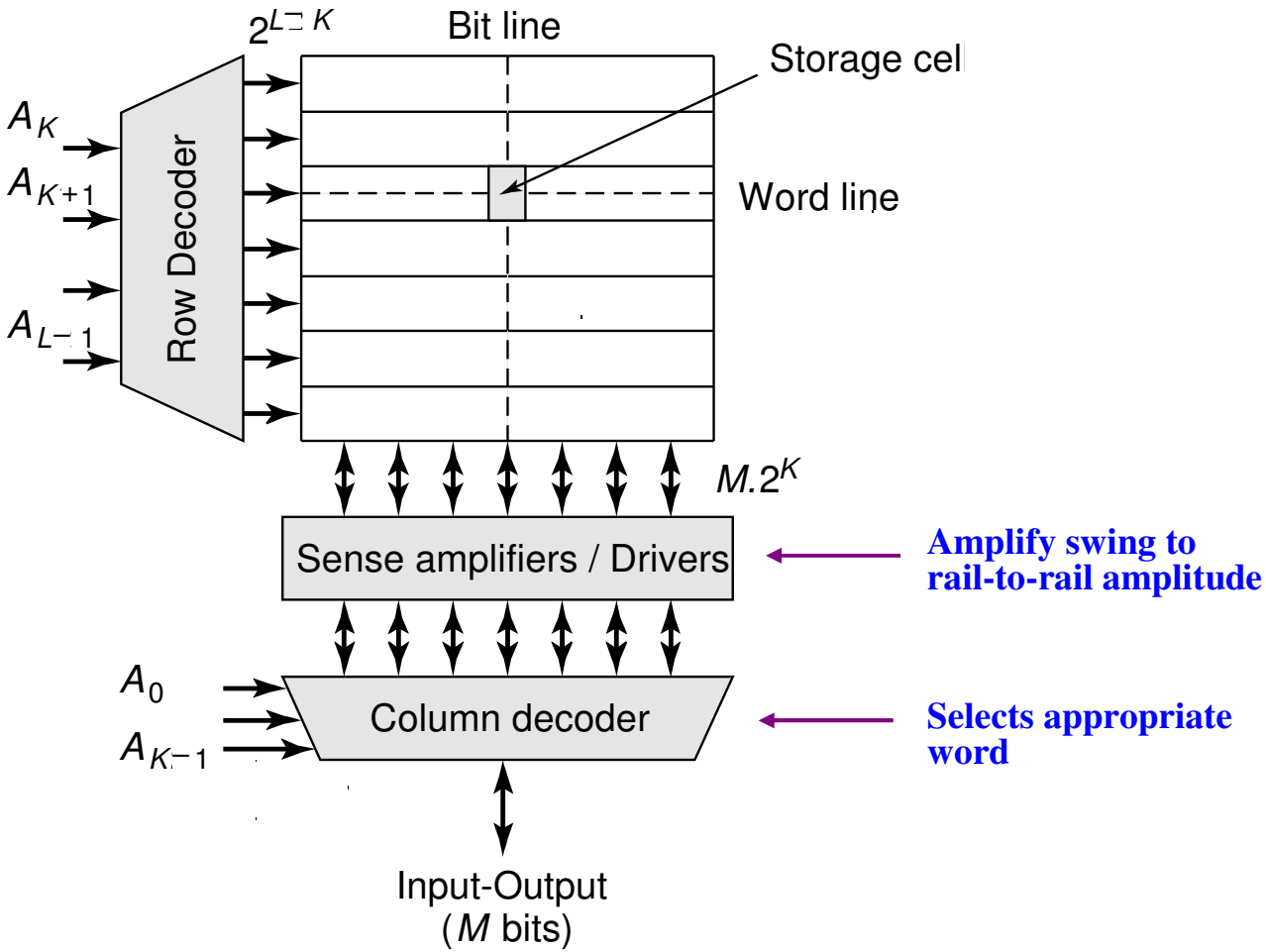
Intuitive architecture for N x M memory
Too many select signals:
N words == N select signals

Decoder reduces the number of select signals

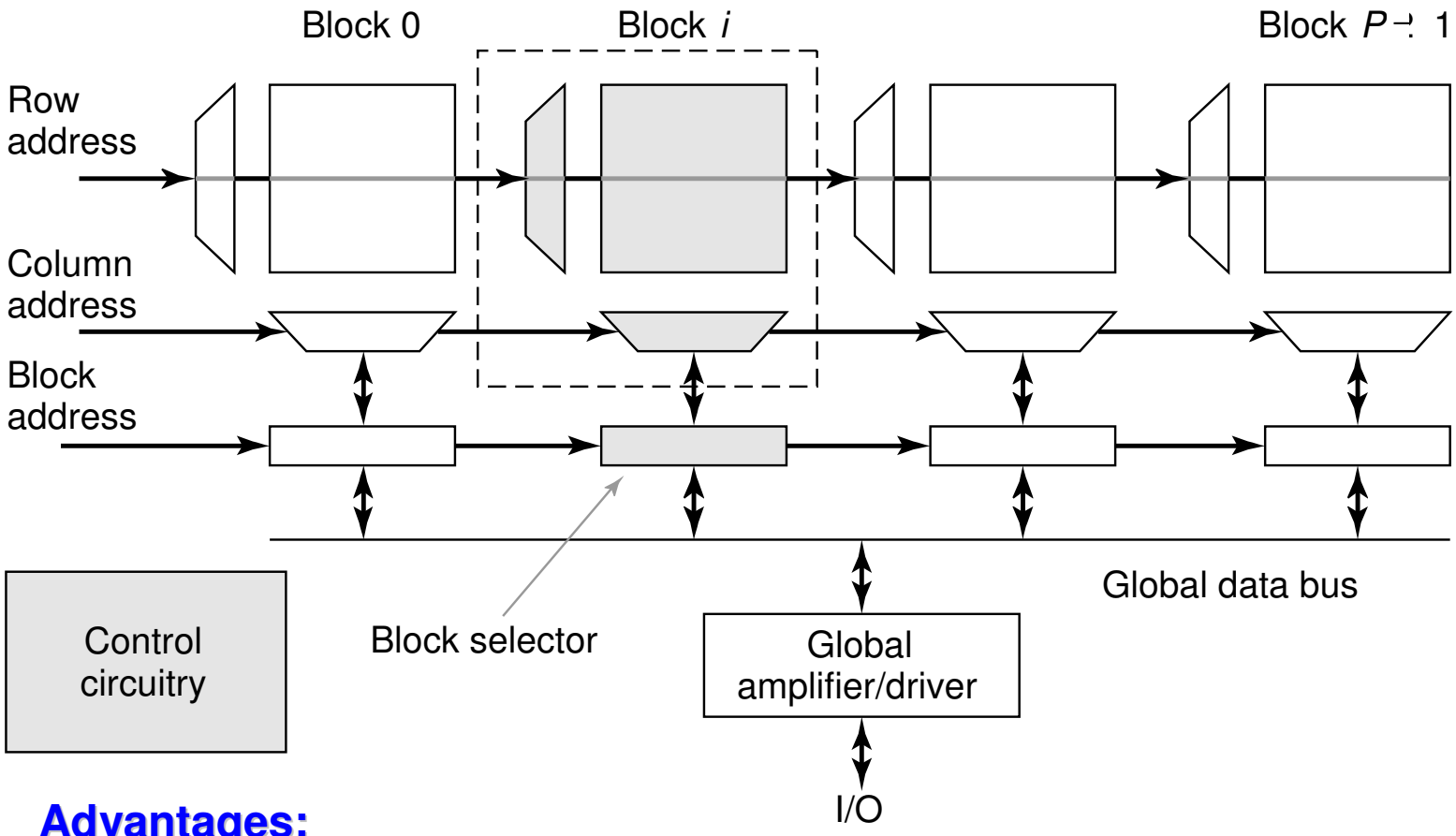
$$K = log_2 N$$

Array-Structured Memory Architecture

Problem: ASPECT RATIO or HEIGHT >> WIDTH



Hierarchical Memory Architecture

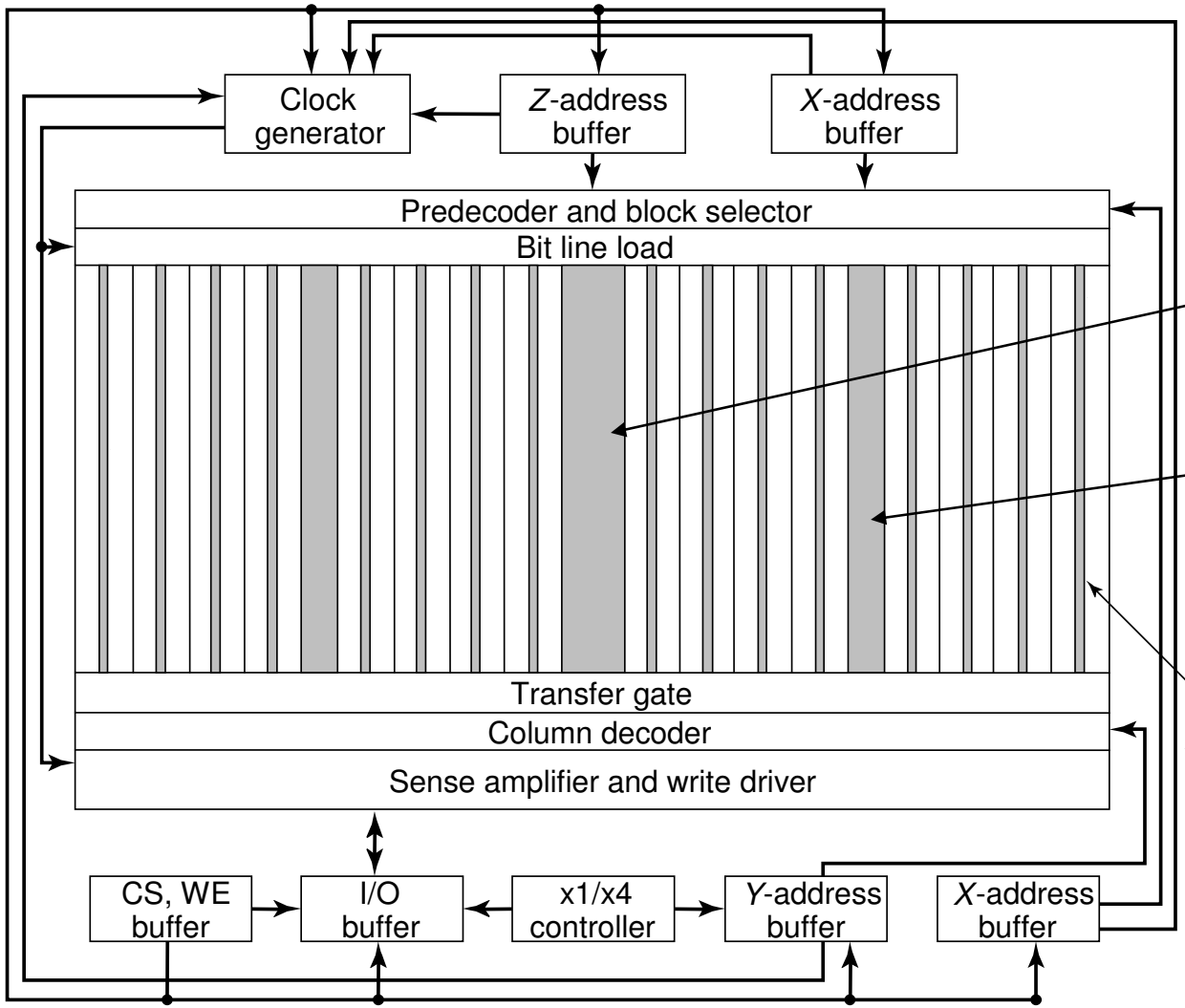


Advantages:

1. Shorter wires within blocks

2. Block address activates only 1 block => power savings

Block Diagram of 4 Mbit SRAM



32 128-bit blocks

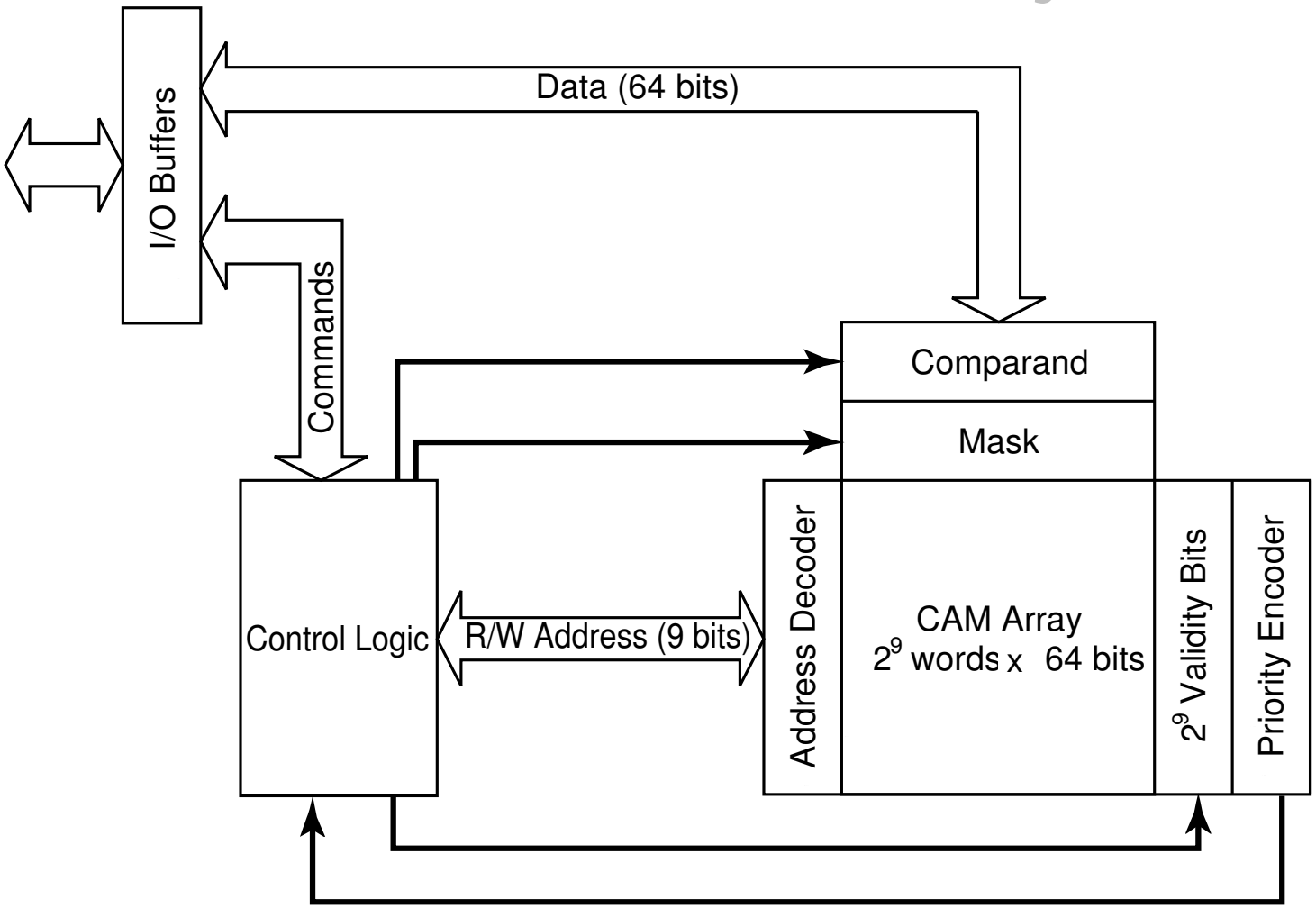
Global row decoder

Sub-global row decoder

Local row decoder

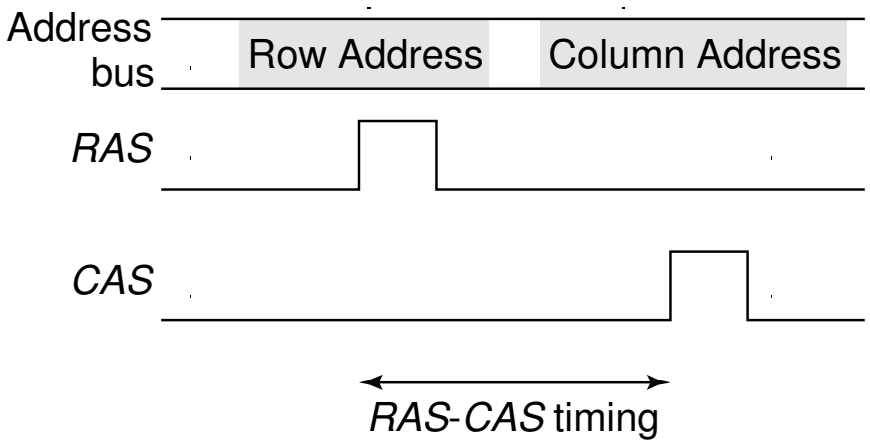
[Hirose90]

Contents-Addressable Memory



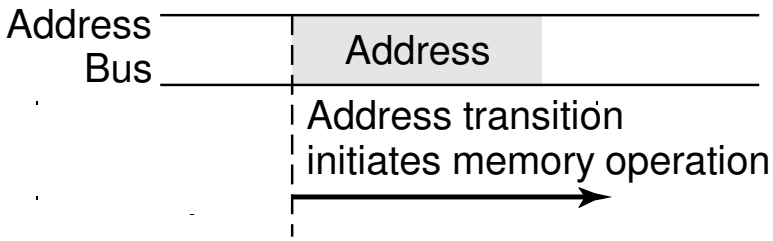
Memory Timing: Approaches

DRAM Timing
Multiplexed Addressing



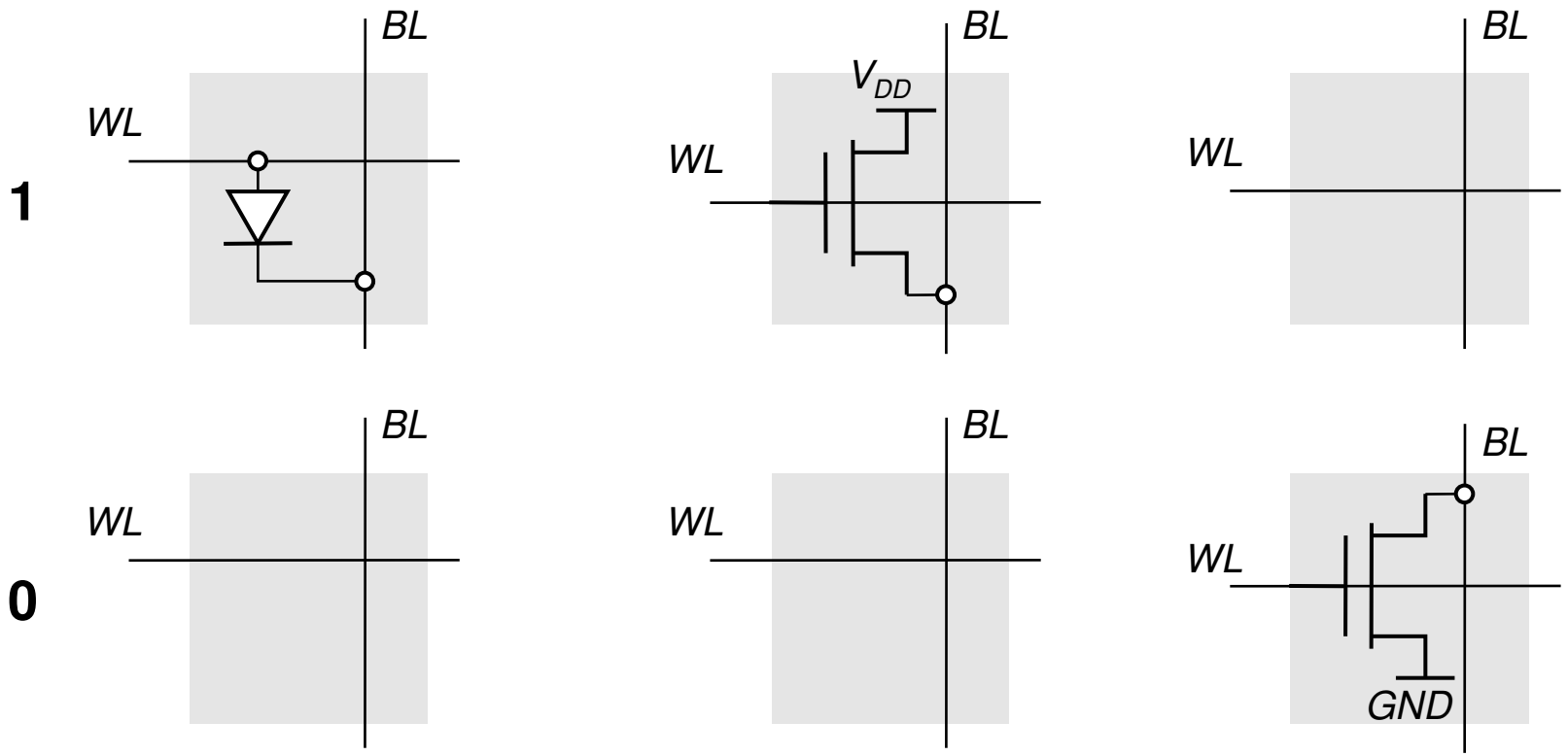
DRAM external timing signals:
RAS= Row Address Strobe
CAS=Column Address Strobe

SRAM Timing
Self-timed



SRAM: no external timing signals!

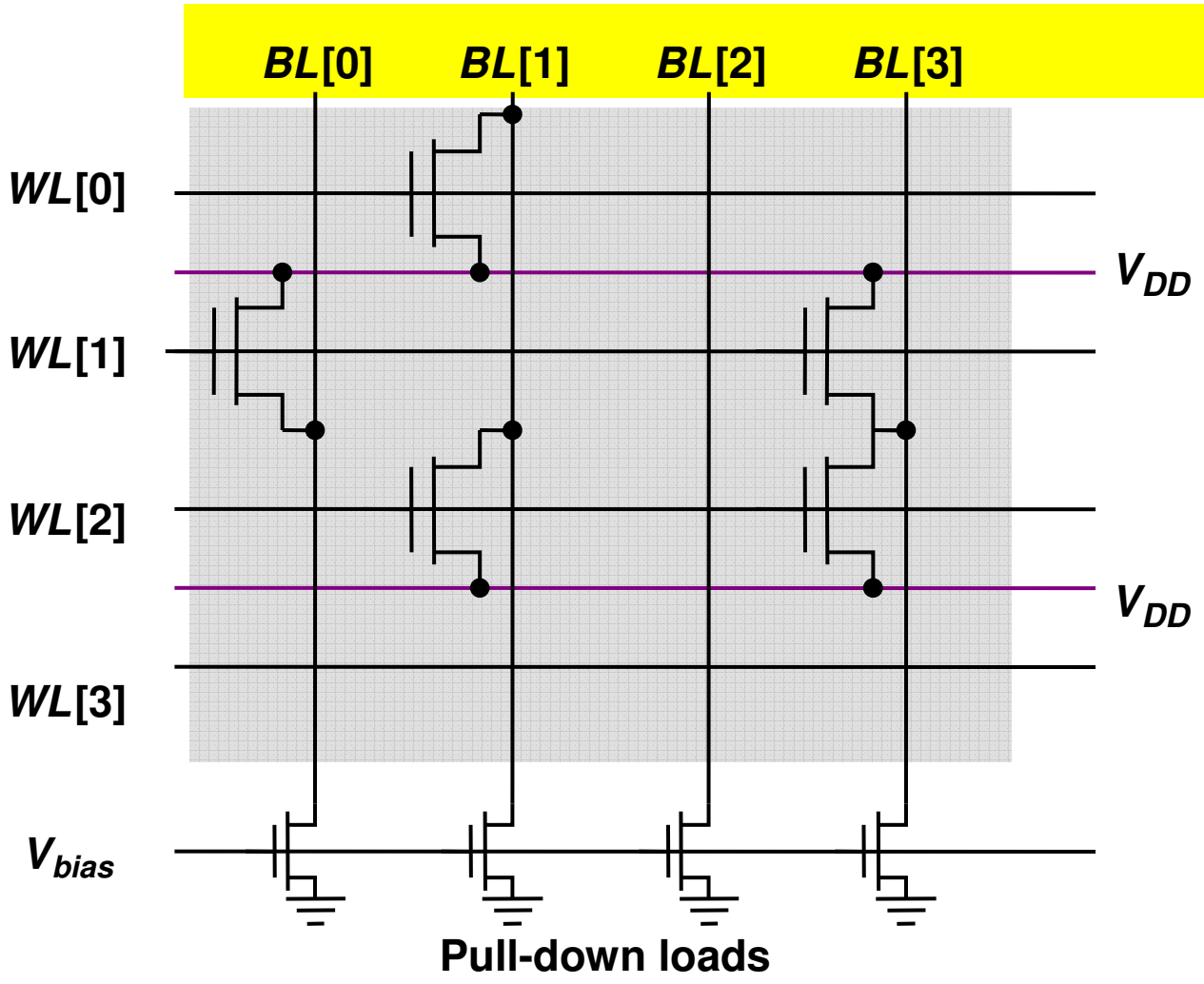
Read-Only Memory Cells



Diode ROM **MOS ROM 1** **MOS ROM 2**

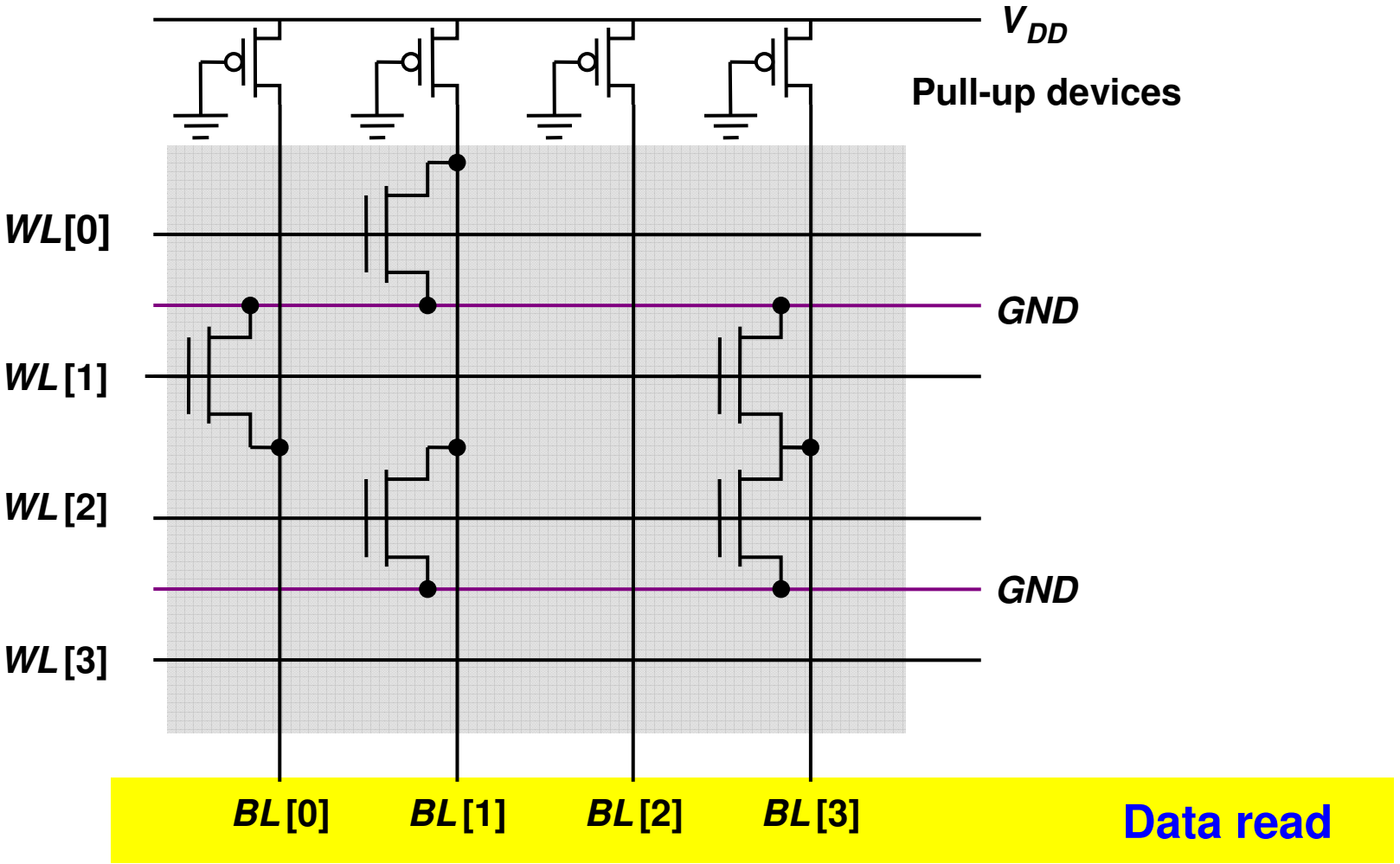
MOS ROM1: BL must be resistively clamped to ground
MOS ROM2: BL must be resistively clamped to Vdd

MOS OR ROM



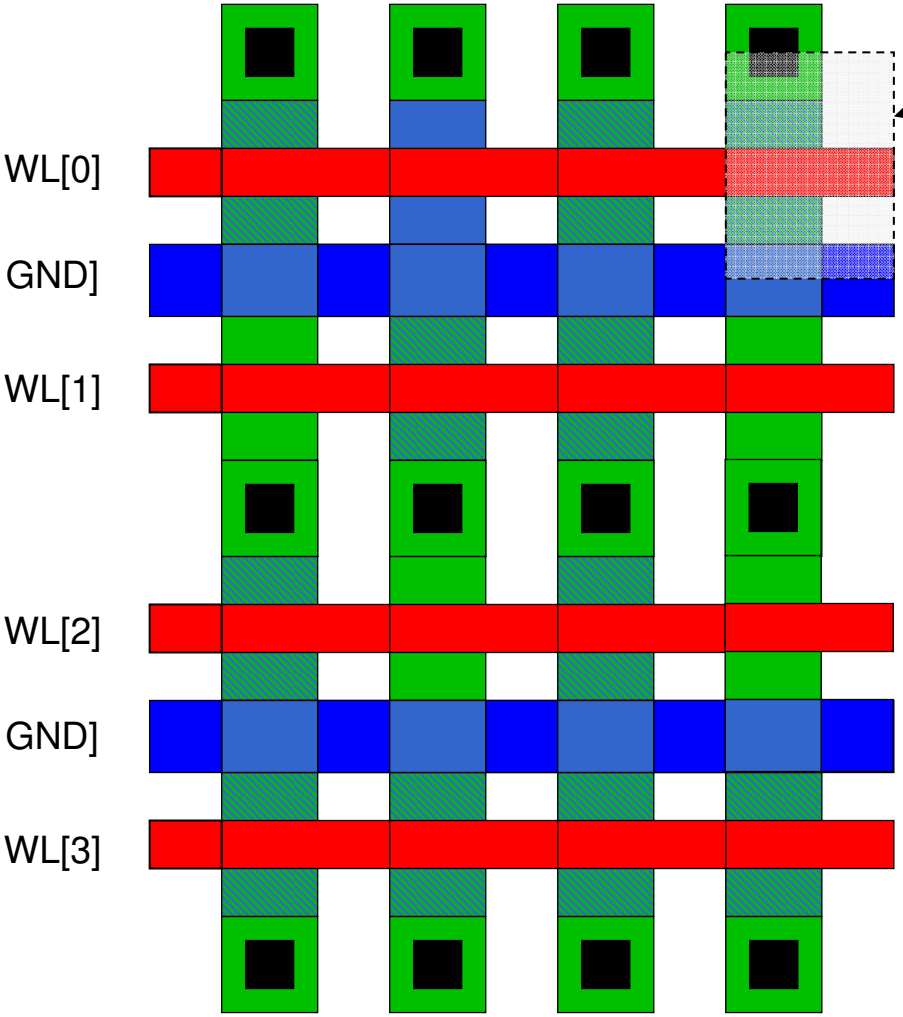
To reduce area overhead, supply voltage lines are shared between adjacent rows

MOS NOR ROM



Each row is a pseudo-NMOS (WLs are the inputs)!

MOS NOR ROM Layout



Cell (9.5λ x 7λ)

Programmming using the Active Layer Only

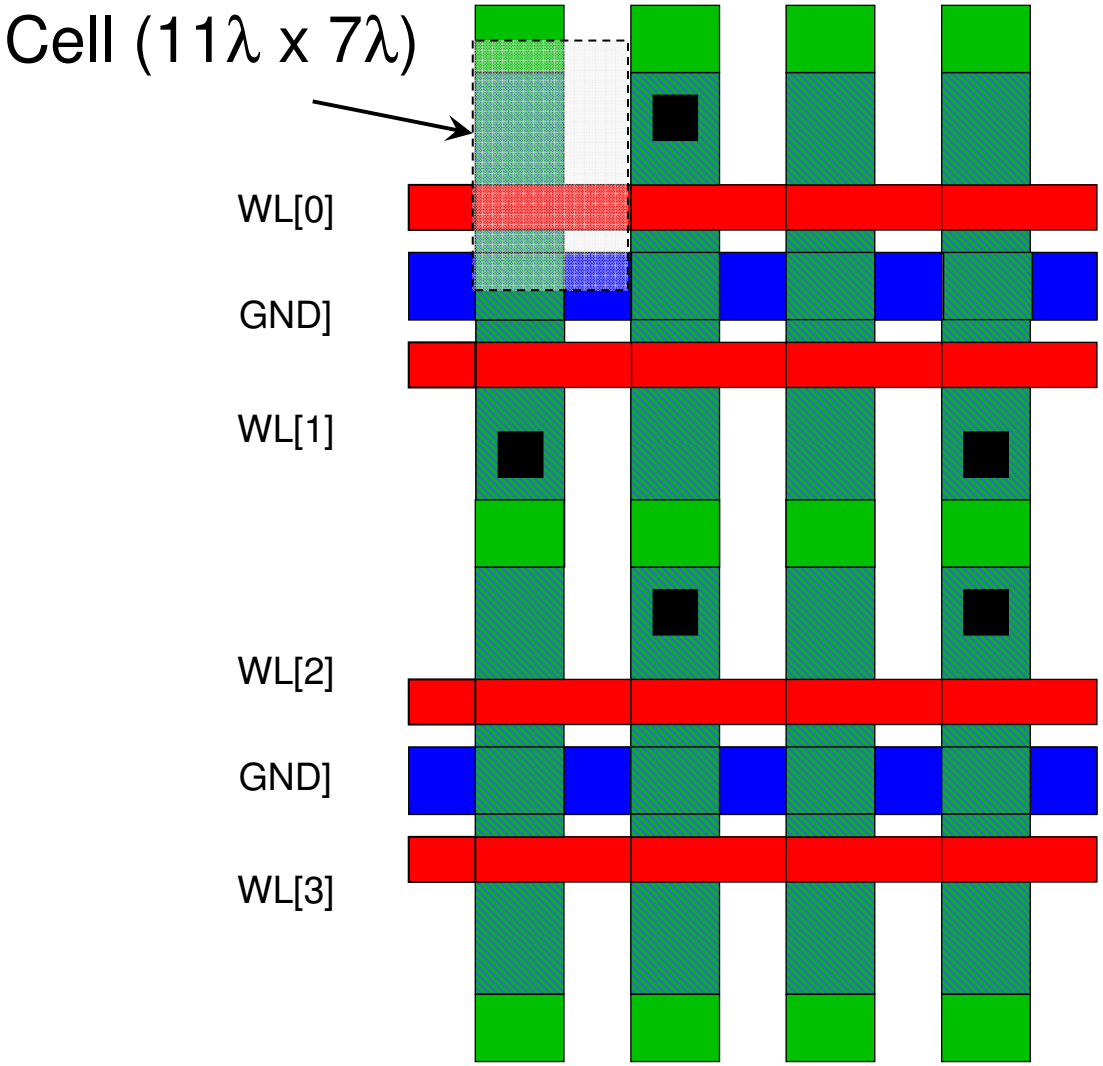
Polysilicon

Metal1

Diffusion

Metal1 on Diffusion

MOS NOR ROM Layout



Programmming using the Contact Layer Only

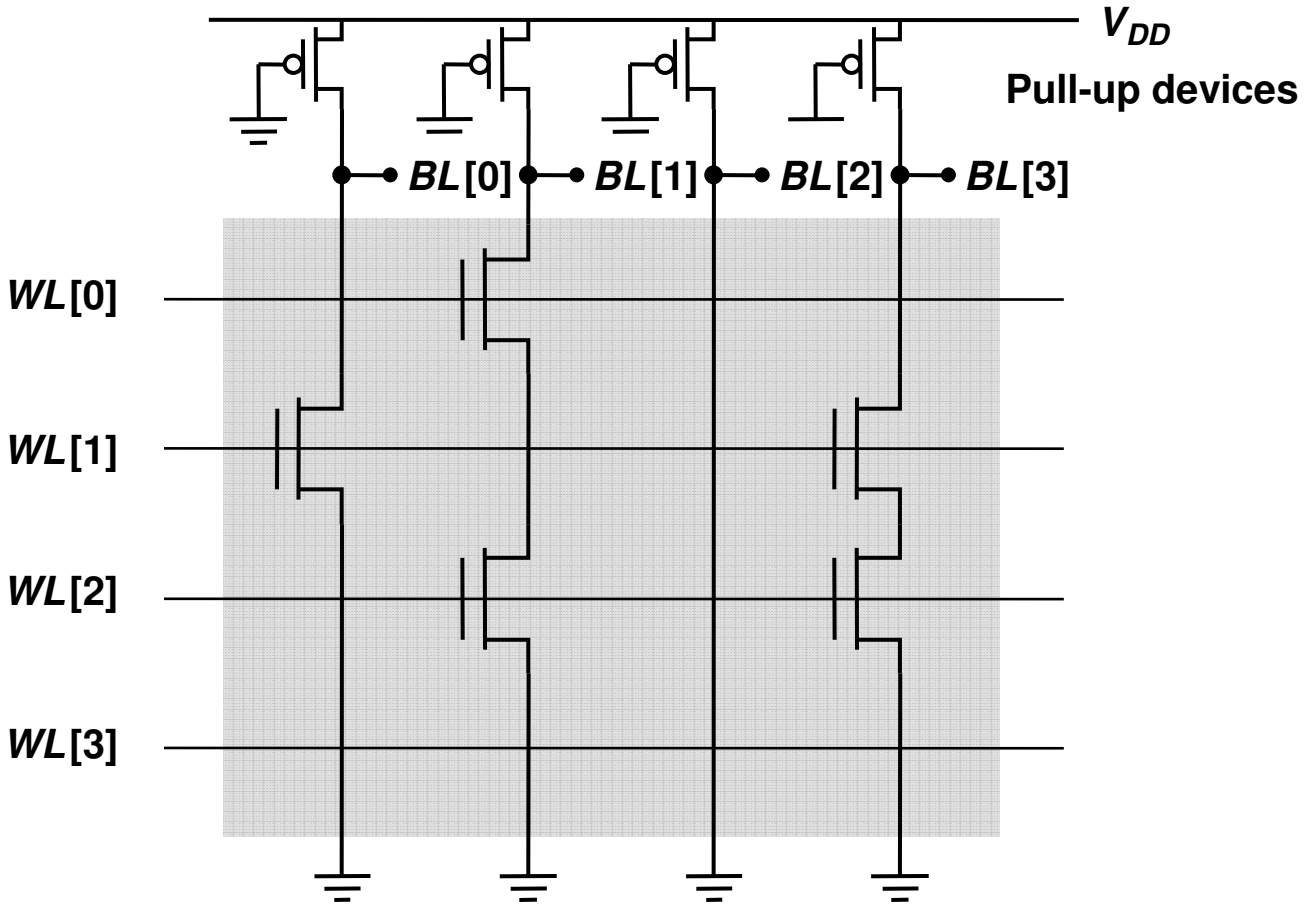
Polysilicon

Metal1

Diffusion

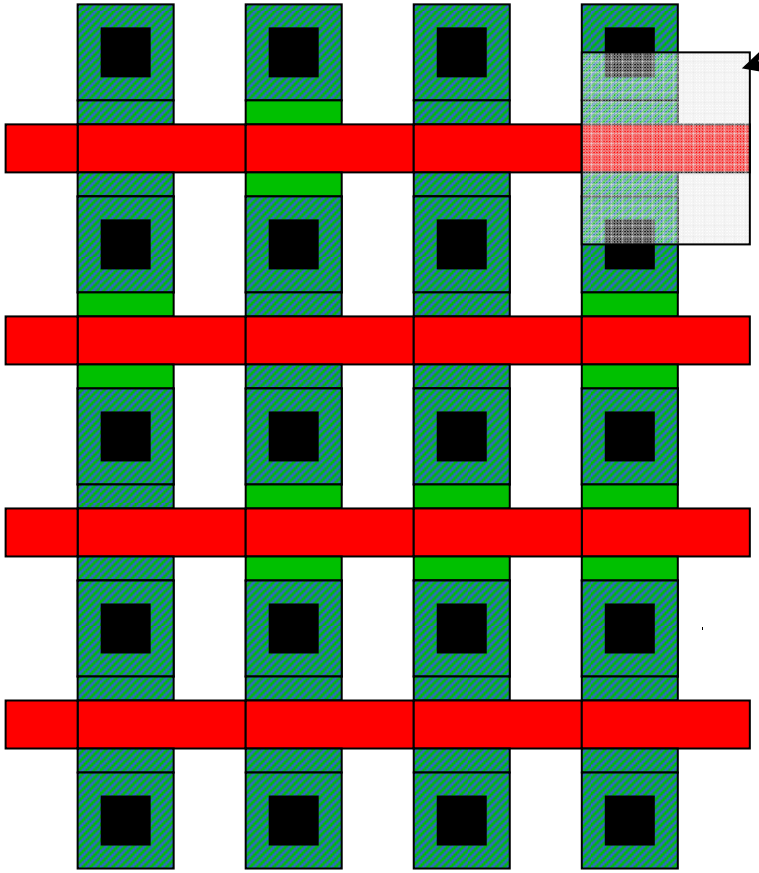
Metal1 on Diffusion

MOS NAND ROM



All word lines high by default with exception of selected row

MOS NAND ROM Layout



Cell (8λ x 7λ)

Programmming using the Metal-1 Layer Only

No contact to VDD or GND necessary;
drastically reduced cell size
Loss in performance compared to NOR ROM

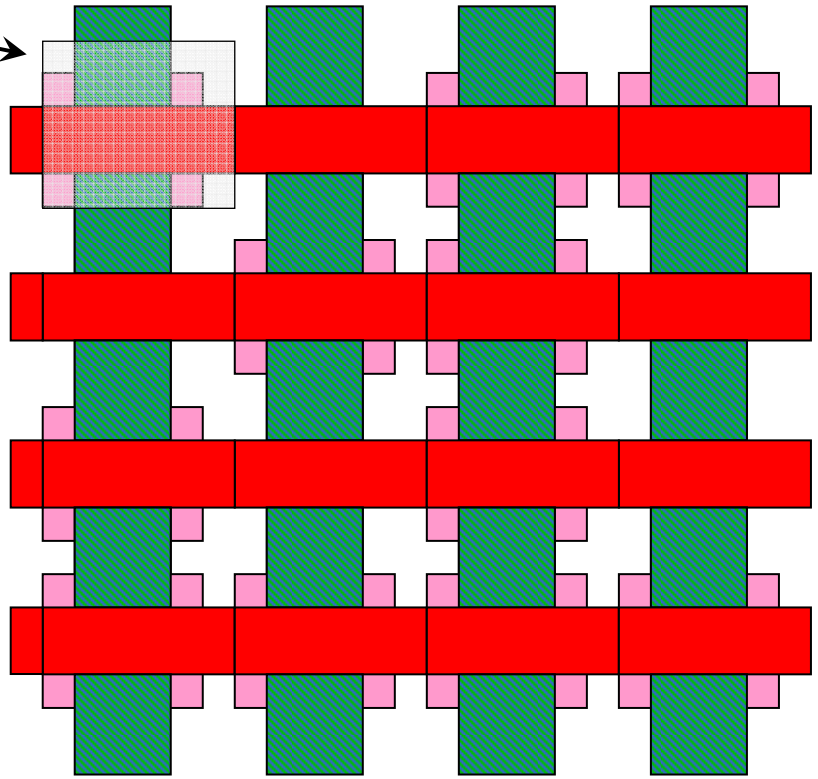
Polysilicon

Diffusion

Metal1 on Diffusion

NAND ROM Layout

Cell (5λ x 6λ)



Programmming using Implants Only

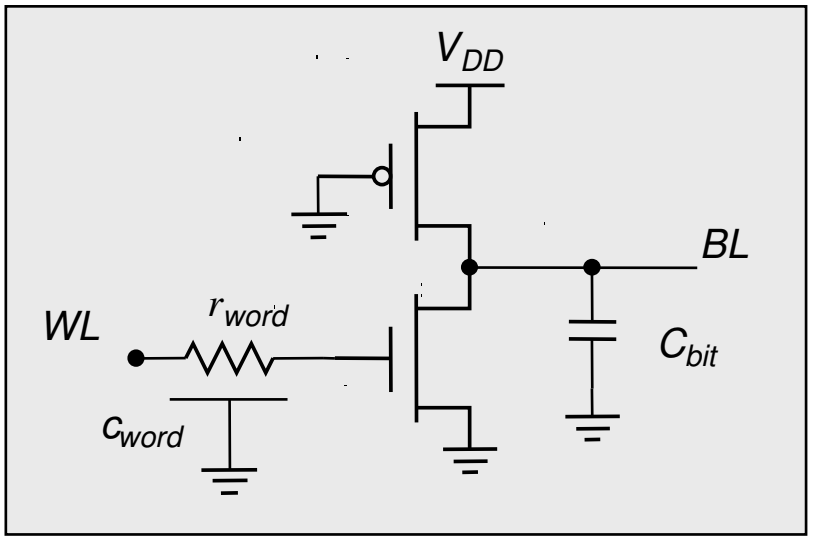
Polysilicon

Threshold-altering implant

Metal1 on Diffusion

Equivalent Transient Model for MOS NOR ROM

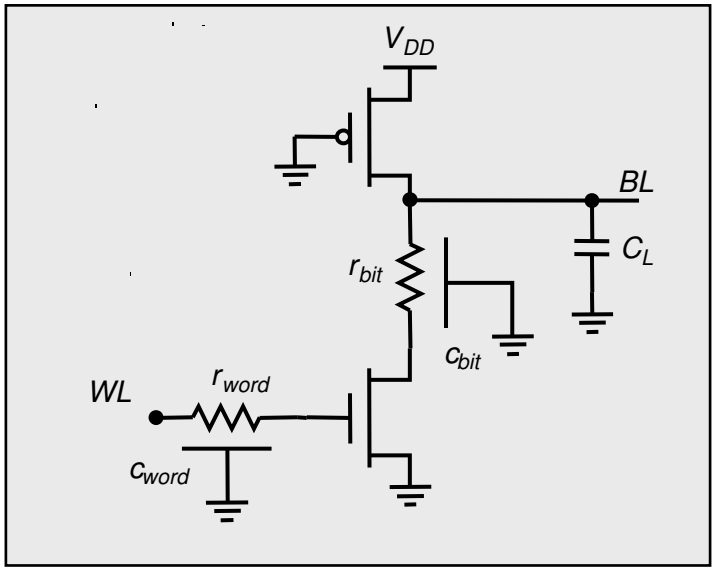
Model for NOR ROM



- Word line parasitics
  - Wire capacitance and gate capacitance
  - Wire resistance (polysilicon)
- Bit line parasitics
  - Resistance not dominant (metal)
  - Drain and Gate-Drain capacitance

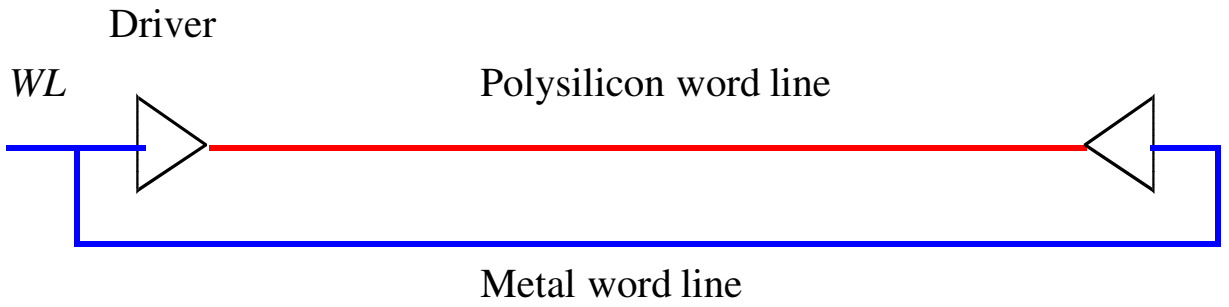
Equivalent Transient Model for MOS NAND ROM

Model for NAND ROM

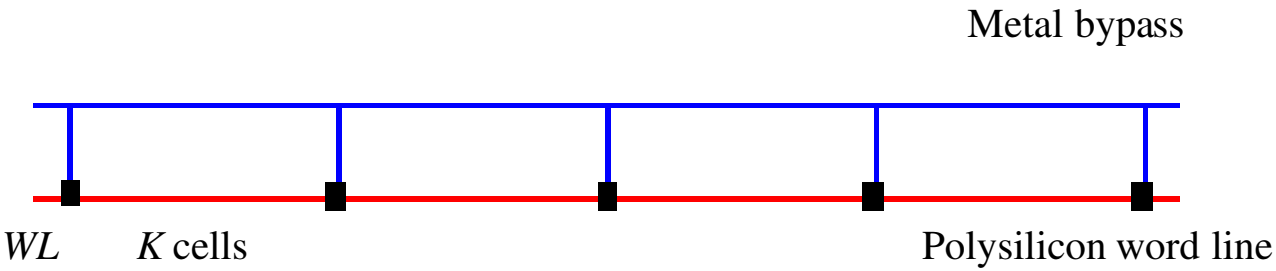


- Word line parasitics
  - Similar to NOR ROM
- Bit line parasitics
  - Resistance of cascaded transistors dominates
  - Drain/Source and complete gate capacitance

Decreasing Word Line Delay



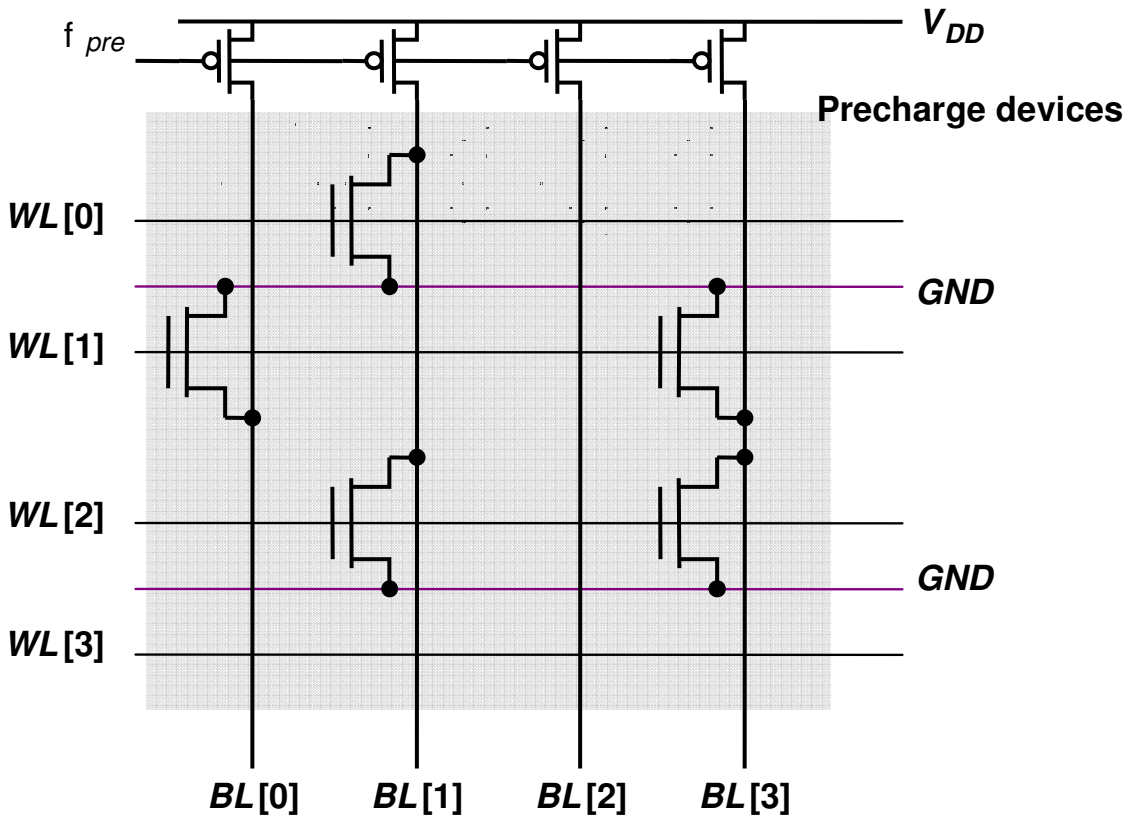
(a) Driving the word line from both sides



(b) Using a metal bypass

(c) Use silicides

Precharged MOS NOR ROM



PMOS precharge device can be made as large as necessary, but clock driver becomes harder to design.