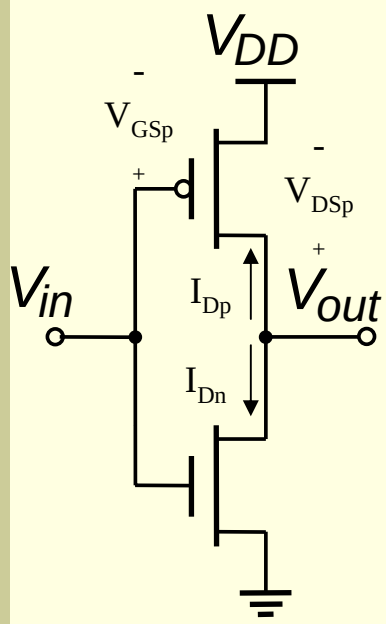
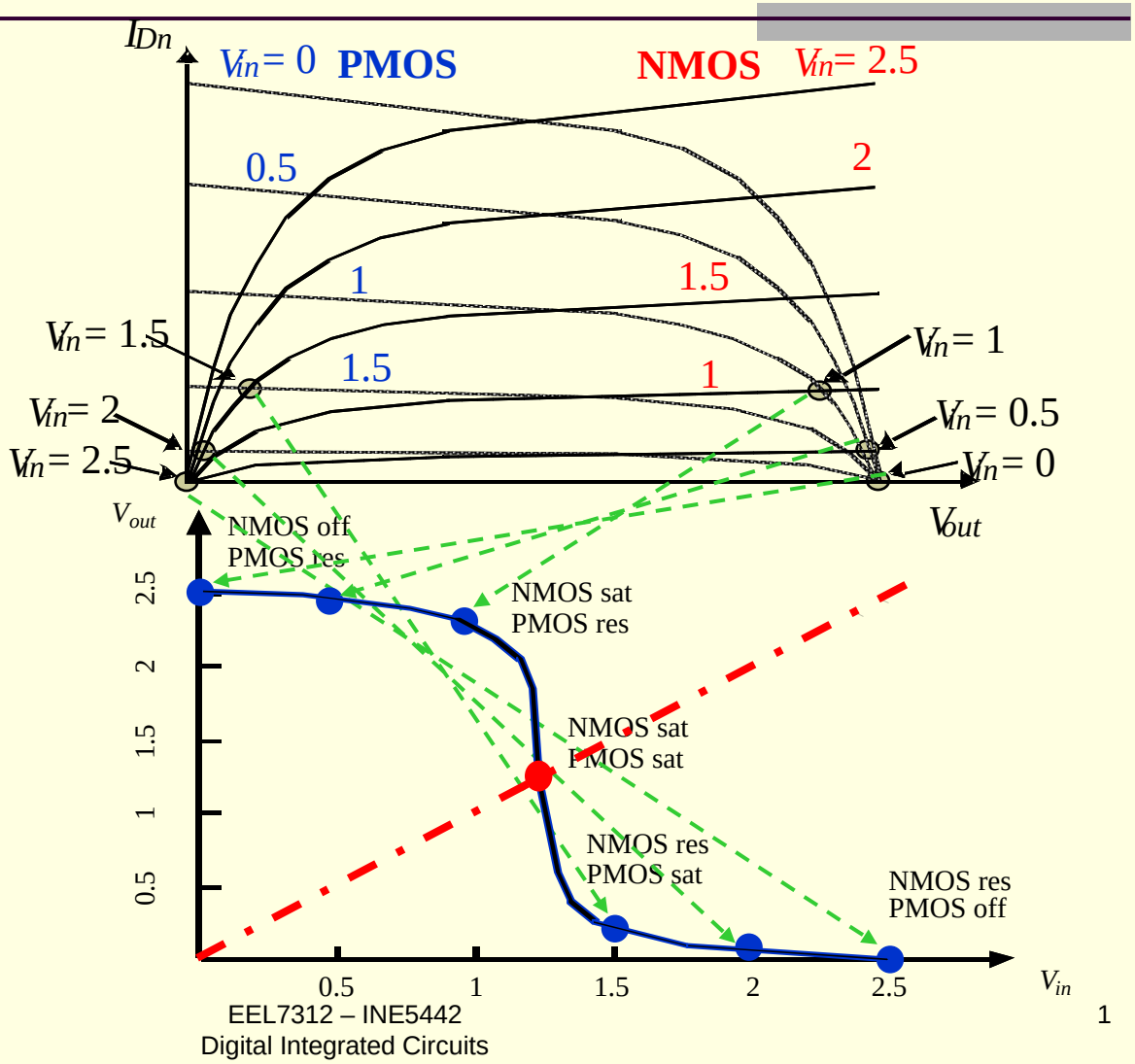
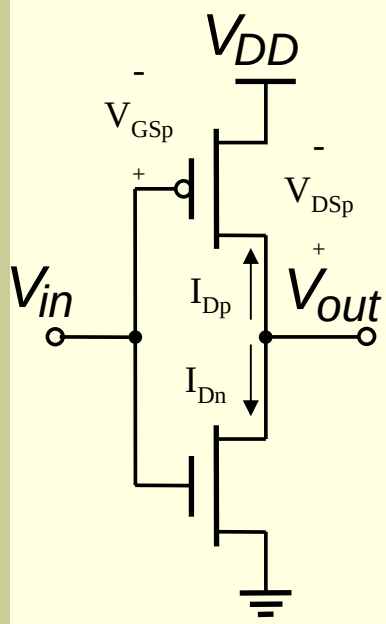
Static characteristics - 4 VTC

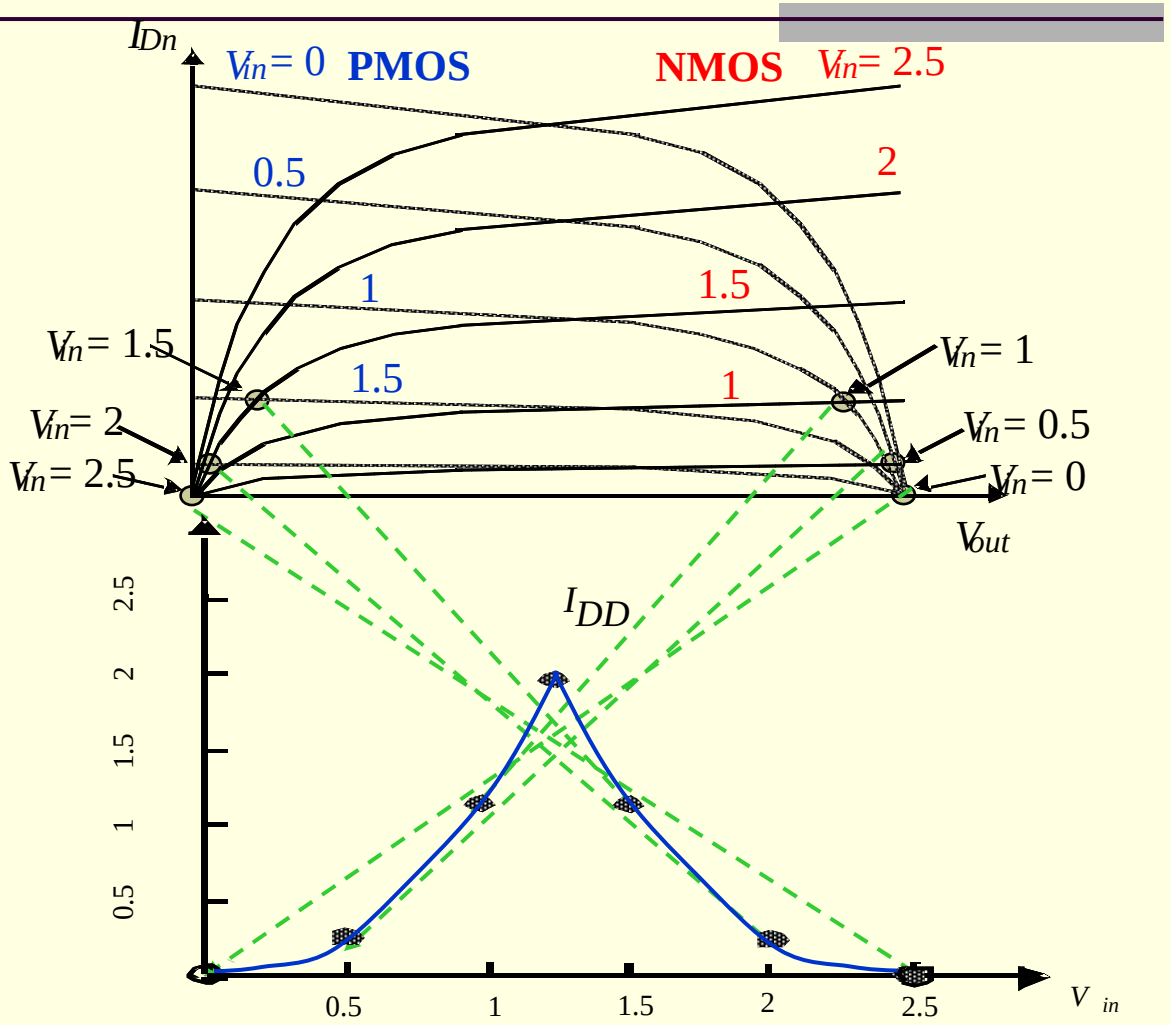




Source: Rabaey

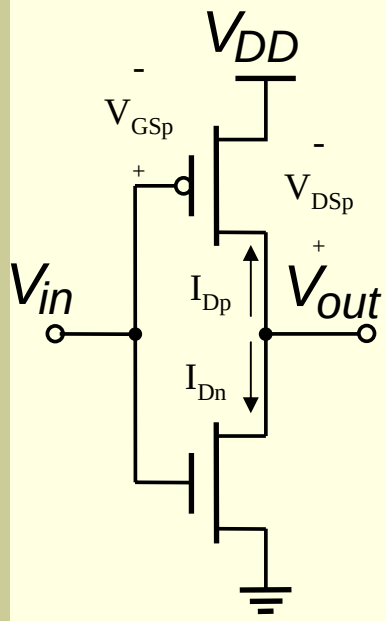
Static characteristics - 5 Short-circuit current

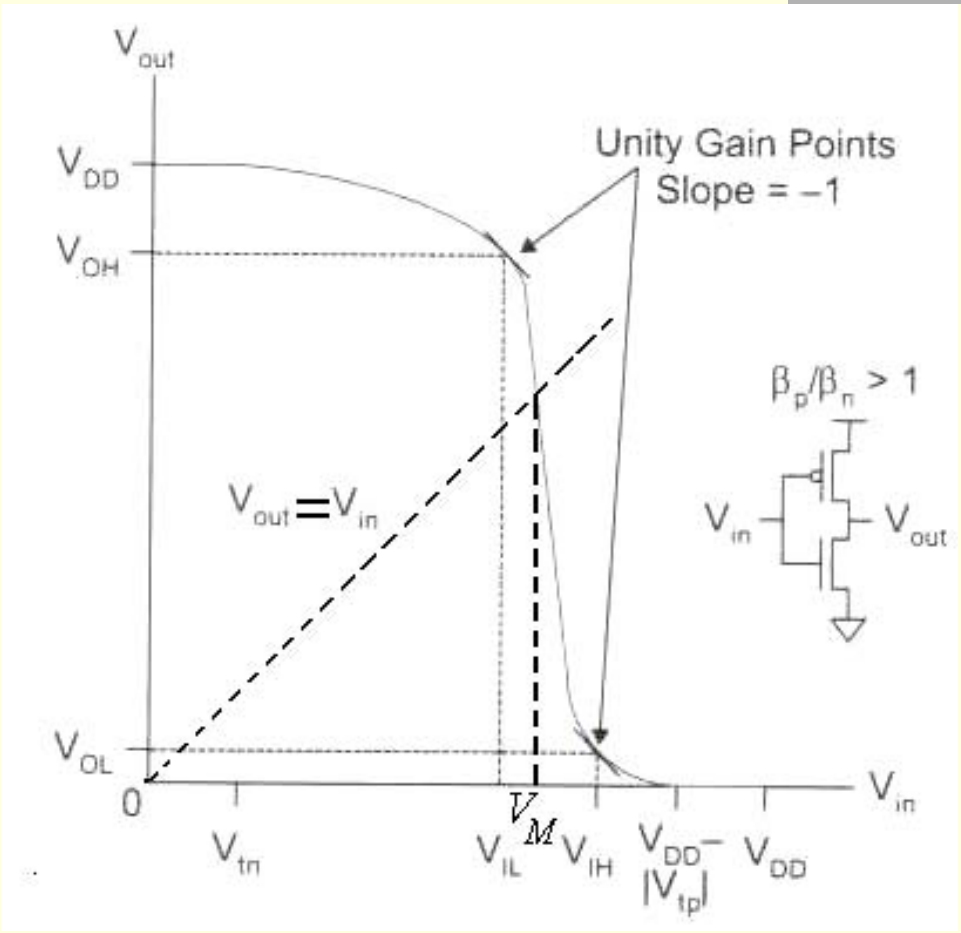




Source: Rabaey

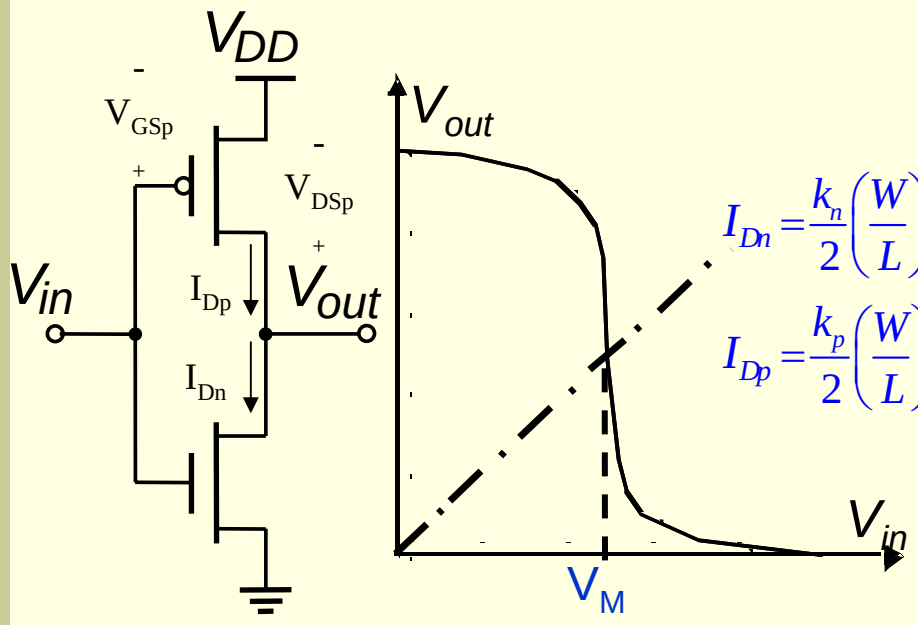
Static characteristics - 6 Switching threshold - 1





Source: Weste & Harris

Static characteristics - 7 Switching threshold - 2



Experimental determination of V_M: short-circuit between input and output

$$I_{Dn} = \frac{k_n}{2}\left(\frac{W}{L}\right)_n \left(V_{GSn} - V_{Tn}\right)^2 \left(1 + \lambda_n V_{DSn}\right) \cong \frac{k_n}{2}\left(\frac{W}{L}\right)_n \left(V_M - V_{Tn}\right)^2$$

$$I_{Dp} = \frac{k_p}{2}\left(\frac{W}{L}\right)_p \left(V_{GSp} - V_{Tp}\right)^2 \left(1 + \lambda_p \left|V_{DSp}\right|\right) \cong \frac{k_p}{2}\left(\frac{W}{L}\right)_p \left(V_{DD} - V_M - \left|V_{Tp}\right|\right)^2$$

Usually $\lambda V_{DS} << 1$

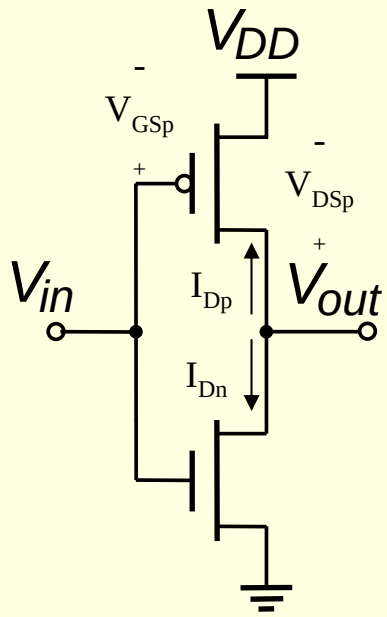
$$I_{Dn} = I_{Dp} \rightarrow V_M = \frac{V_{Tn} + rV_{Tp}}{1+r} + \frac{rV_{DD}}{1+r};$$

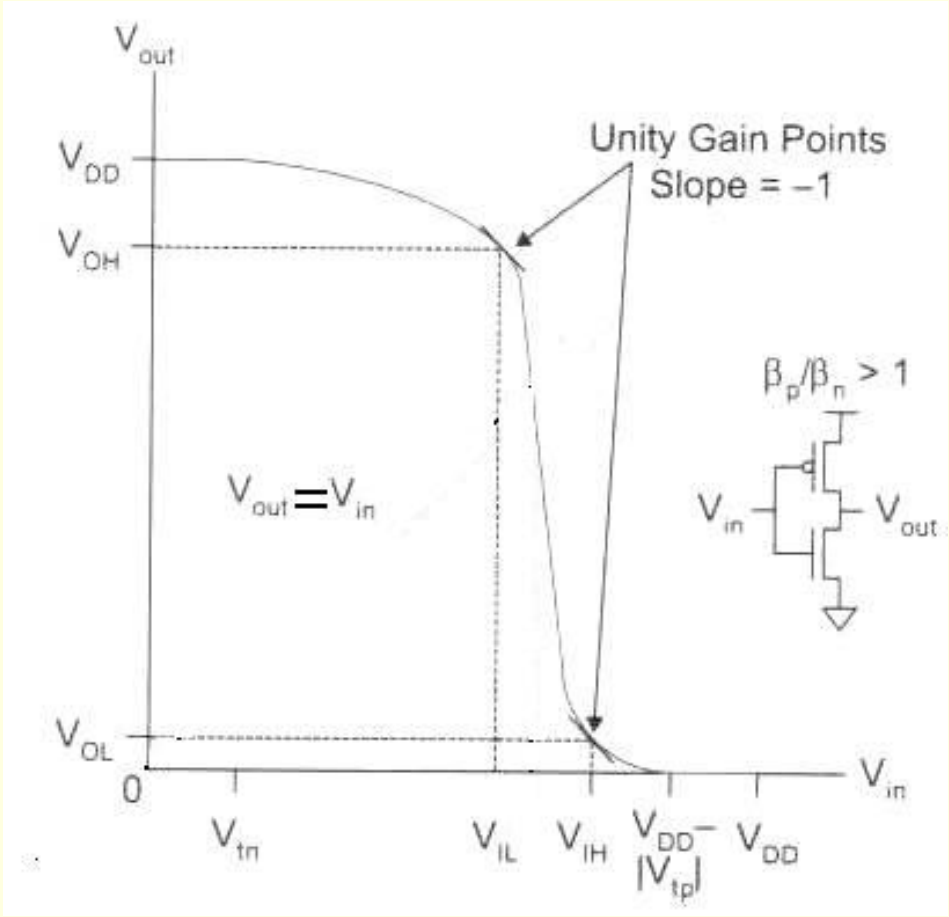
$$r = \sqrt{\frac{k_p}{k_n}\frac{\left(W/L\right)_p}{\left(W/L\right)_n}}$$

Example: V_{DD}=2.5 V, V_{Tp}=-0.4 V, V_{Tn}=0.43 V. What is V_M for r= 0.5, 1.0, and 1.5? Answer: V_M=0.98, 1.26, and 1.43 V, respectively.

Source: Weste & Harris

Static characteristics - 8 Noise margins - 1

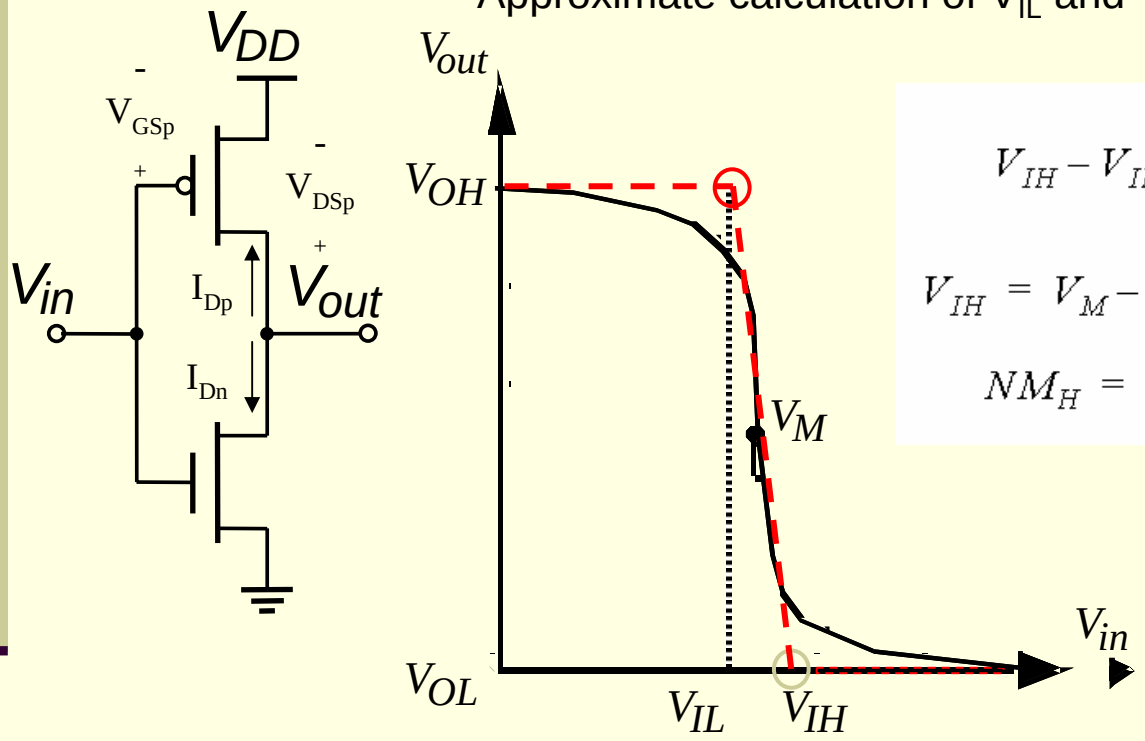




Source: Weste & Harris

Static characteristics - 9 Noise margins - 2

Approximate calculation of V_{IL} and V_{IH}



$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

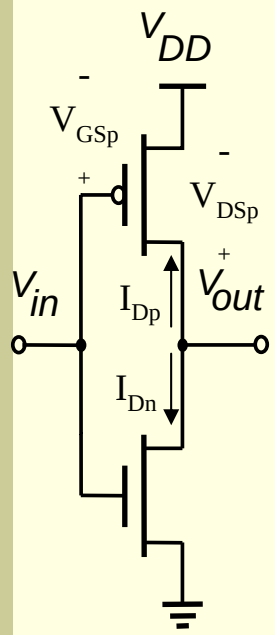
$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

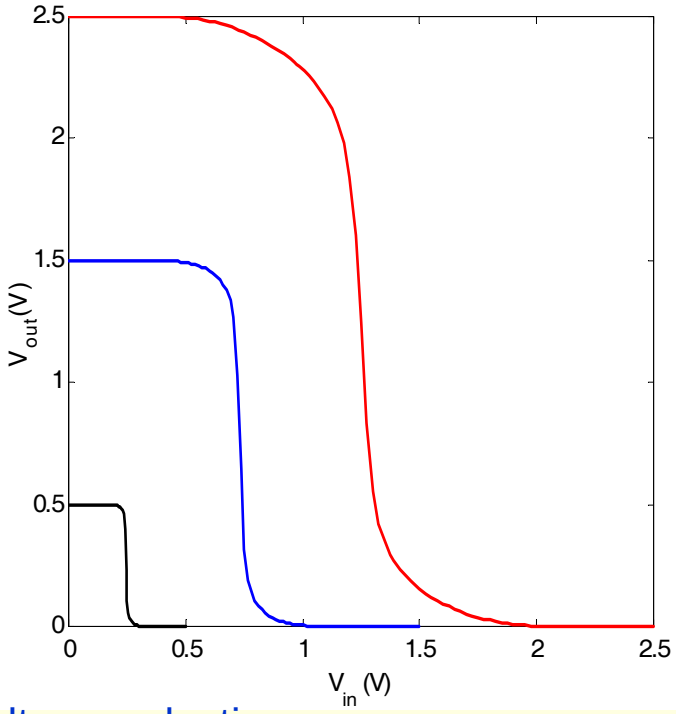
$$NM_H = V_{DD} - V_{IH} \qquad NM_L = V_{IL}$$

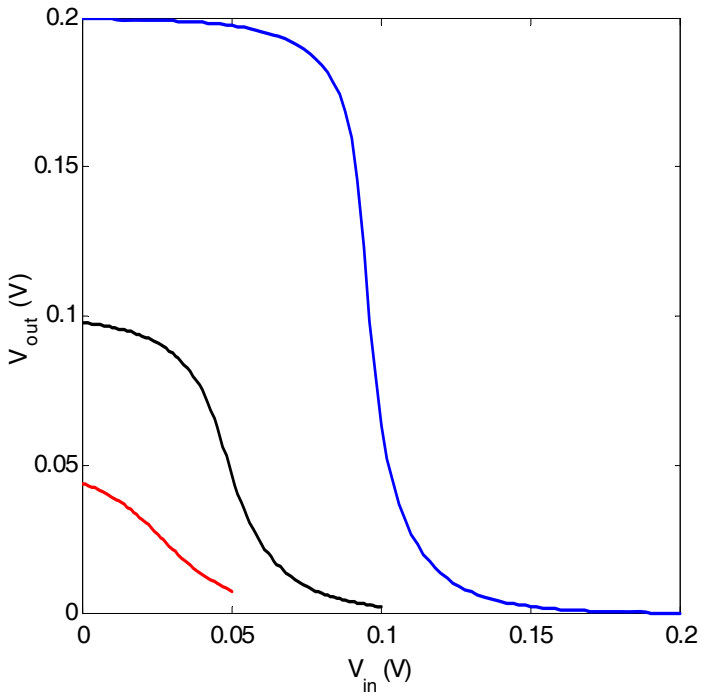
For regeneration *-g>1,* g is the gain in transition region

Source: Rabaey

Static characteristics - 10 Scaling the supply voltage





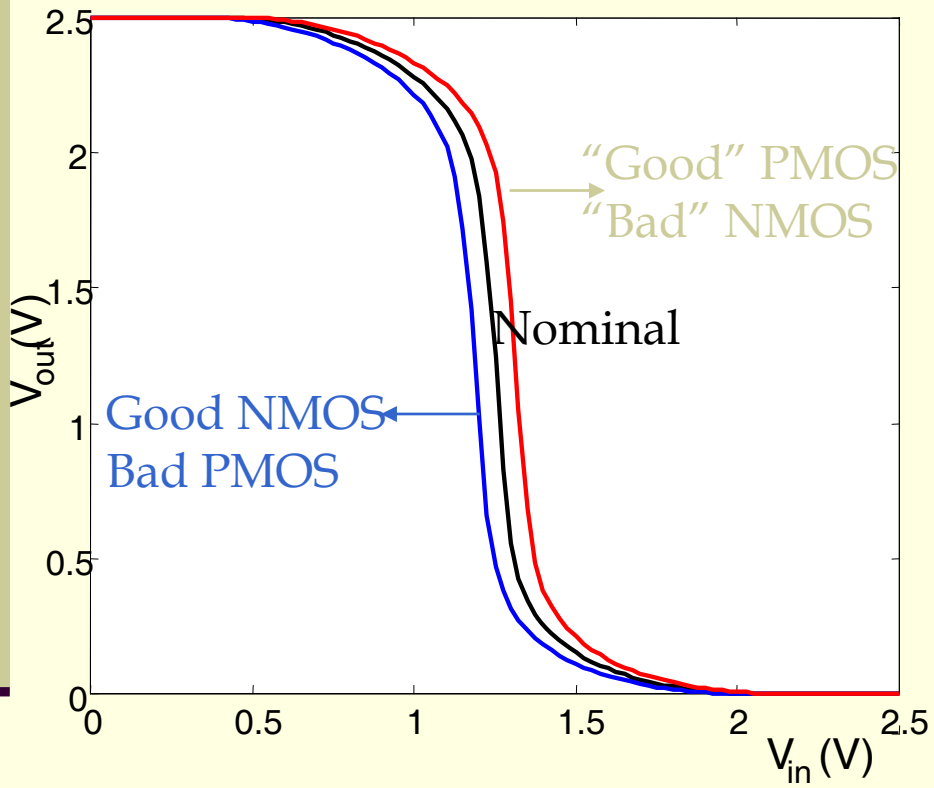


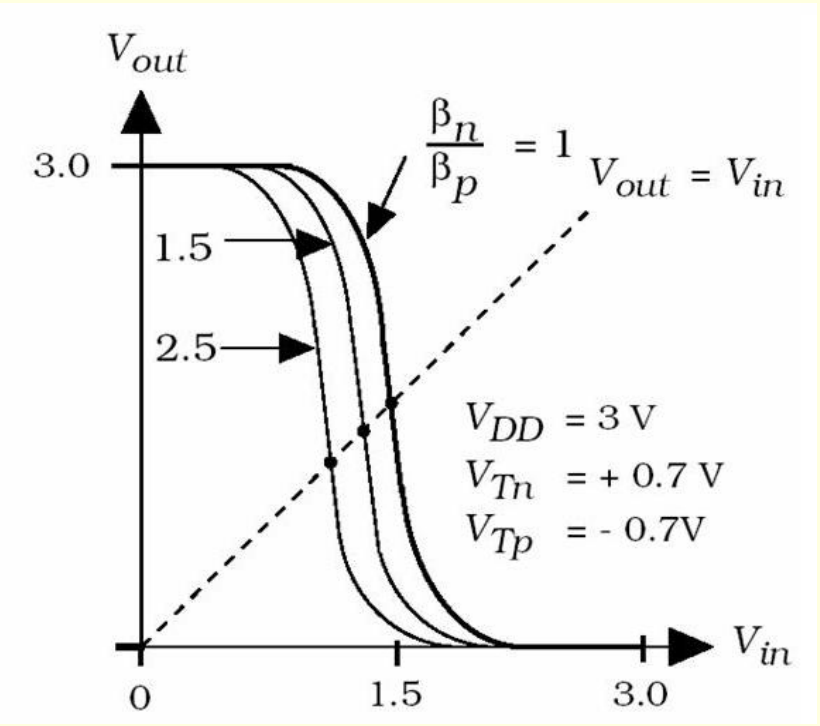
Effects of supply voltage reduction:

- Energy dissipation decreases but gate delay increases
- dc characteristic becomes more sensitive to variations in device parameters
- Signal swing reduces making the design more sensitive to external noise sources that do not scale

Source: Rabaey

Static characteristics -11 Impact of Process Variations





Notes:

1. $k'_n \approx 2$ to 3 k'_p
2. For $\beta_n=\beta_p$ and $V_{Tp}=-V_{Tn}$, $V_M=V_{DD}/2$

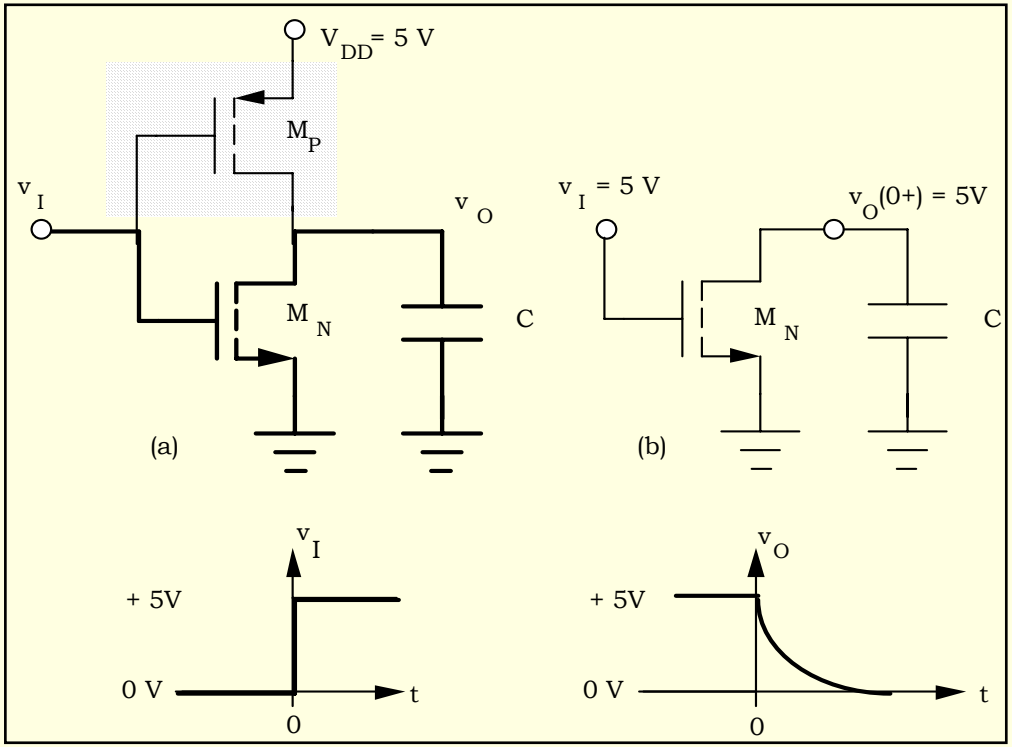
$$\beta = k' \frac{W}{L}$$

Source: Rabaey

Source: Uyemura

Dynamic operation - 1

High-to-low output transition in a CMOS inverter

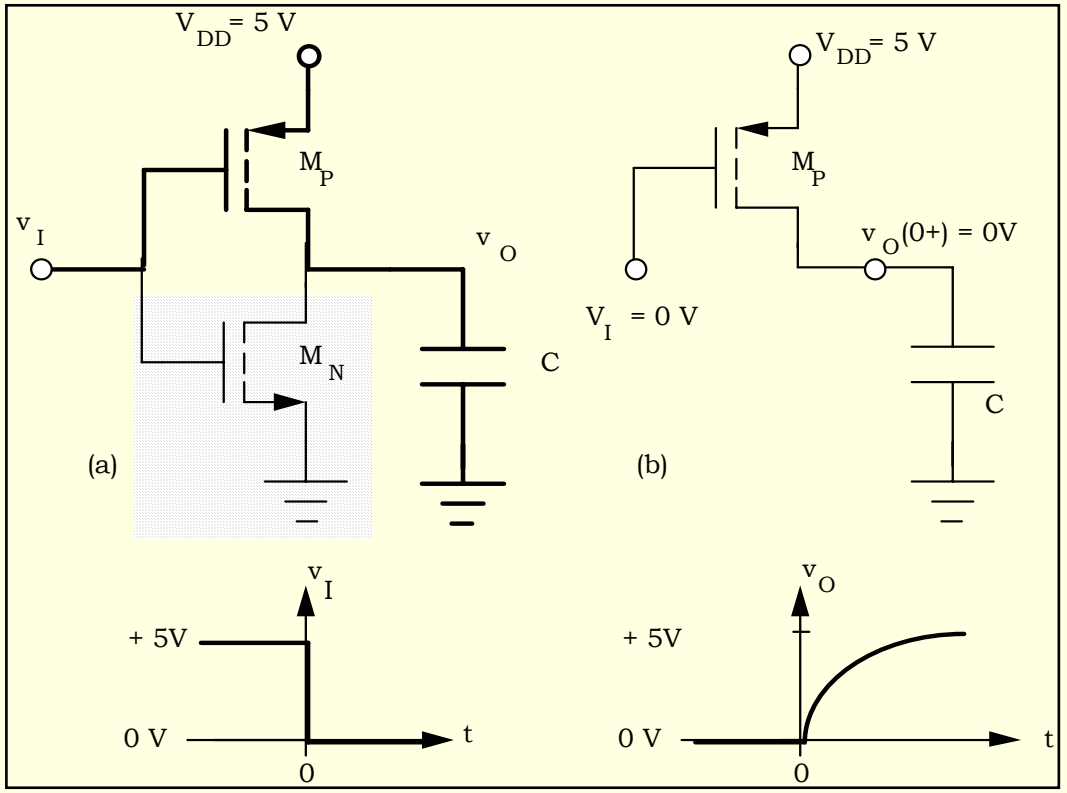


C: load capacitance + interconnect capacitance + capacitances associated with the inverter transistors

Source: Jaeger

Dynamic operation - 2

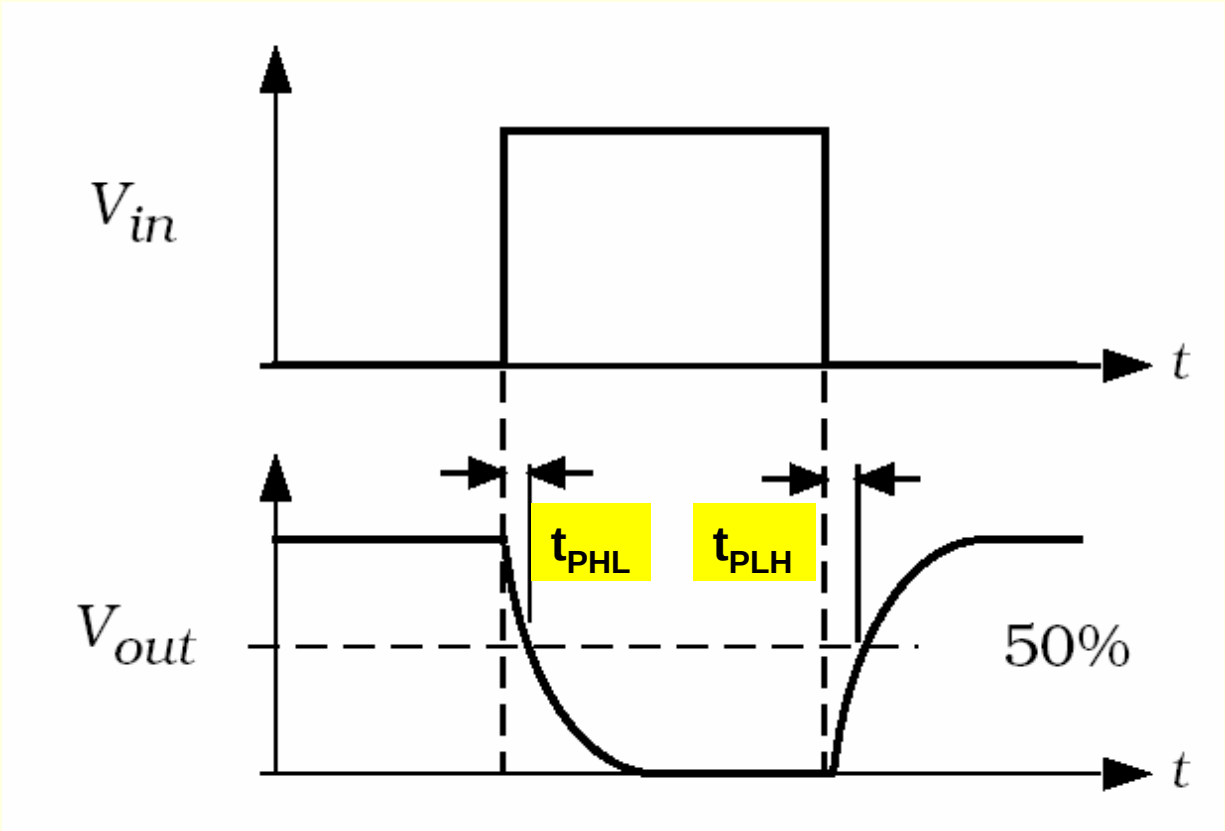
Low-to- high output transition in a CMOS inverter



C: load capacitance + interconnect capacitance + capacitances associated with the inverter transistors

Source: Jaeger

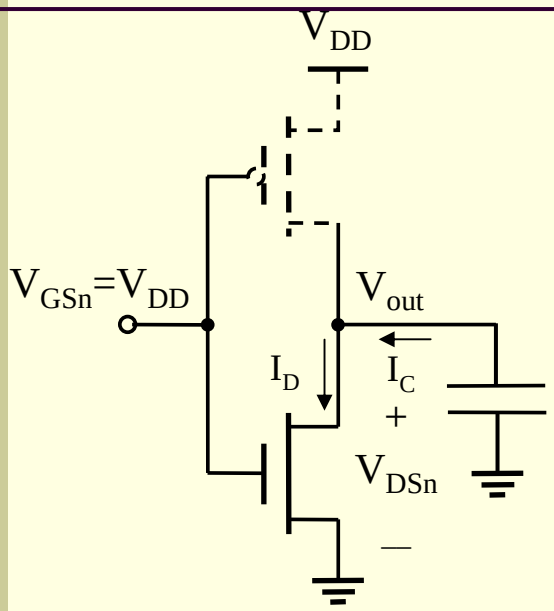
Dynamic operation - 3

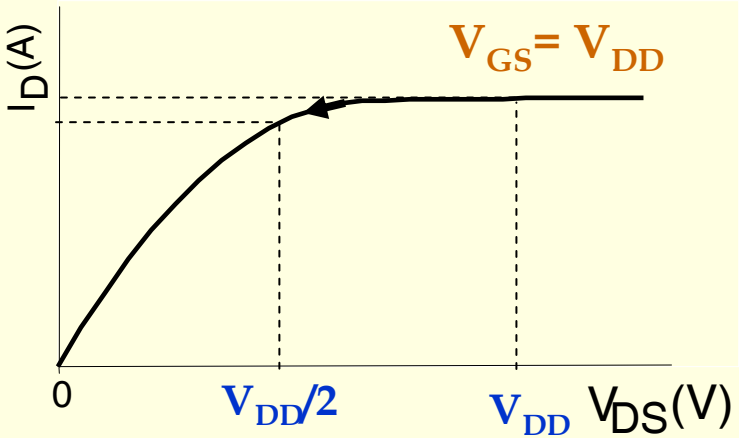


Source: Uyemura

Dynamic operation - 4

Propagation delay - 1





$$I_D = I_C = -C\frac{dV_{out}}{dt}$$

$$t = 0 \rightarrow V_{out} = V_{DD}$$

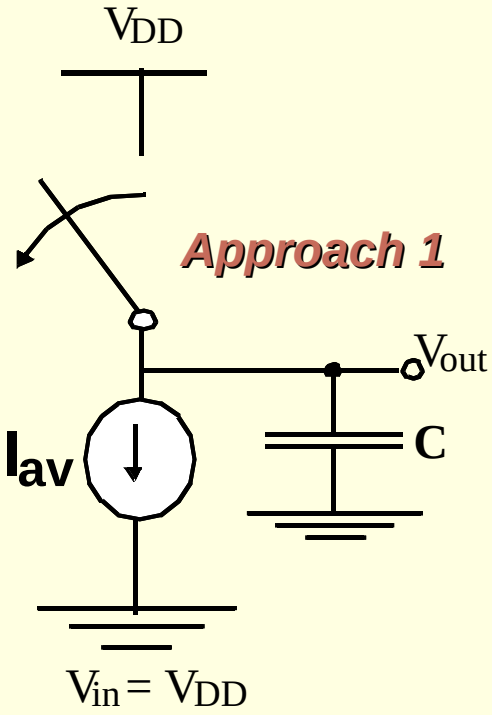
$$t = t_{PHL} \rightarrow V_{out} = V_{DD}/2$$

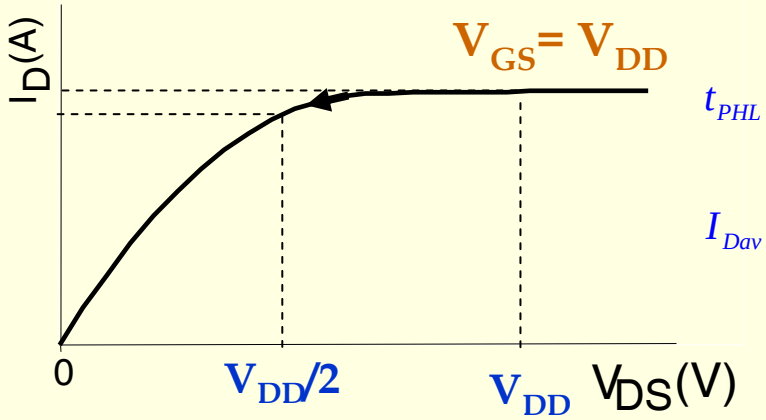
$$\int_0^{t_{PHL}} dt = -\int_{V_{DD}}^{V_{DD}/2} C\frac{dV_{out}}{I_D} \rightarrow t_{PHL} = \frac{CV_{DD}/2}{I_{Dav}}$$

$$I_{Dav} = \frac{1}{V_{DD}/2}\int_{V_{DD}/2}^{V_{DD}} I_D(V_{DS})\,dV_{DS}$$

Dynamic operation - 5

Propagation delay - 2





$$t_{PHL} = \frac{CV_{DD}/2}{I_{Dav}}$$

$$I_{Dav} = \frac{1}{V_{DD}/2}\int_{V_{DD}/2}^{V_{DD}} I_D(V_{DS})\,dV_{DS}$$

$$I_D \cong \frac{k_n}{2}\left(\frac{W}{L}\right)_n (V_{GS}-V_{Tn})^2 \text{ for } V_{DS} > V_{GS}-V_{Tn}$$

$$I_D \cong k_n\left(\frac{W}{L}\right)_n \left[(V_{GS}-V_{Tn})V_{DS} - V_{DS}^2/2\right] \text{ for } V_{DS} \le V_{GS}-V_{Tn}$$

Let us assume that $I_{Dav} \cong I_{Dsat} = \frac{k_n}{2}\left(\frac{W}{L}\right)_n (V_{DD}-V_{Tn})^2$ and that $V_{DD} >> V_{Tn}$

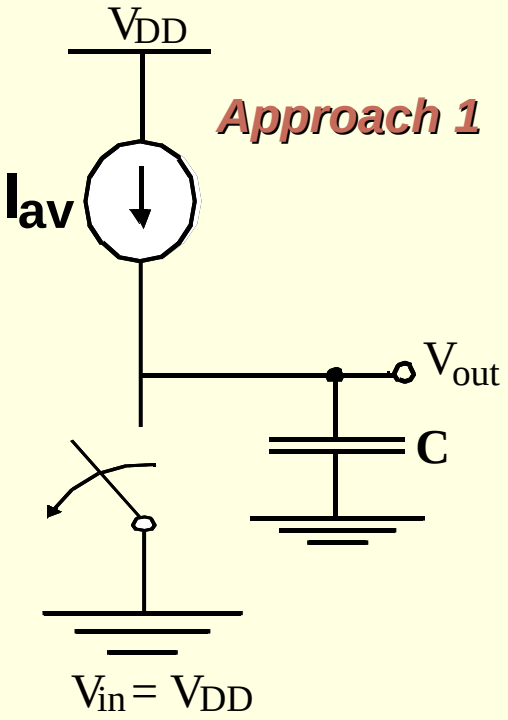
In this case we have $t_{PHL} = \frac{CV_{DD}/2}{I_{Dav}} \approx \frac{CV_{DD}/2}{\frac{k_n}{2}\left(\frac{W}{L}\right)_n (V_{DD}-V_{Tn})^2}$;

$$t_{PHL} \approx \frac{C}{k_n\left(\frac{W}{L}\right)_n V_{DD}}$$

Source: Rabaey

Dynamic operation - 6

Propagation delay - 3



$$I_{Dav} \cong I_{Dsat} = \frac{k_p}{2}\left(\frac{W}{L}\right)_p \left(V_{DD} + V_{Tp}\right)^2 \text{ and that } V_{DD} >> -V_{Tp}$$

$$t_{PLH} = \frac{CV_{DD}/2}{I_{Dav}} \approx \frac{CV_{DD}/2}{\frac{k_p}{2}\left(\frac{W}{L}\right)_n \left(V_{DD} + V_{Tp}\right)^2}; \quad t_{PLH} \approx \frac{C}{k_p\left(\frac{W}{L}\right)_p V_{DD}}$$

$$t_P = \frac{t_{PLH} + t_{PHL}}{2}$$

$$t_{PHL} \approx \frac{C}{k_n\left(\frac{W}{L}\right)_n V_{DD}}$$

Comments:

- ***$k_n \approx 2\text{-}3\ k_p$, $k_{n,p} = \mu_{n,p} \cdot C_{ox}$***
- ***Increasing V_{DD} reduces t_p but power goes up***
- ***t_{PLH} can be $\approx t_{PHL}$ by making $(W/L)_p \approx 2\text{-}3(W/L)_n$ BUT C is dependent on transistor dimensions***
- ***C includes load (fan-out), wire, inverter "self-capacitance"***
- ***C is non linear***

Source: Rabaey

Dynamic operation - 7

Propagation delay - 4

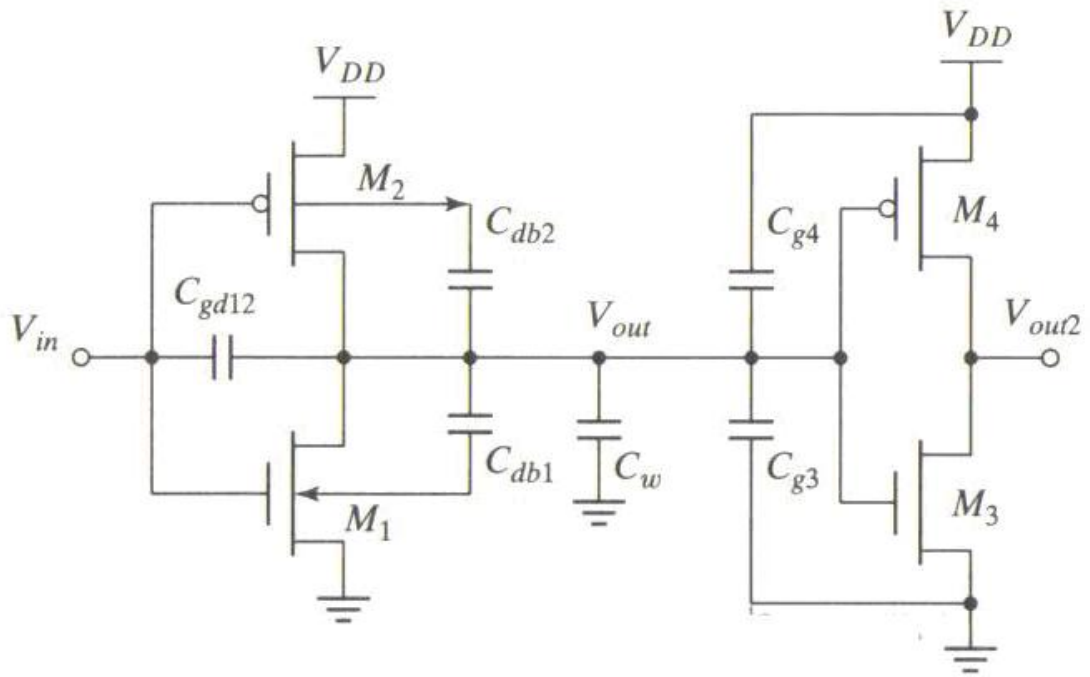
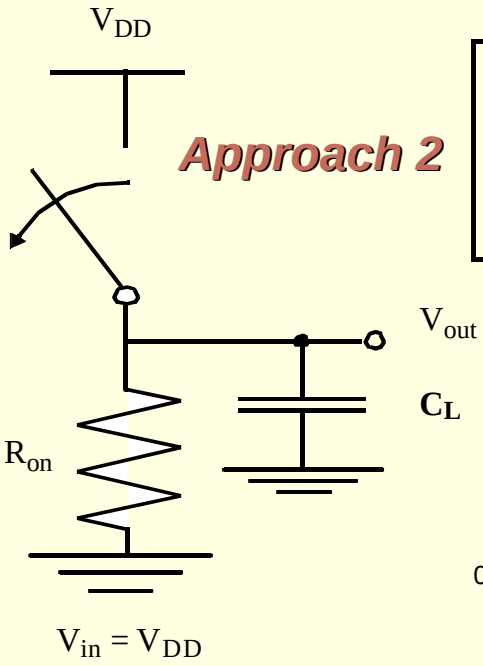


Figure 5-13 Parasitic capacitances, influencing the transient behavior of the cascaded inverter pair.

Source: Rabaey

Dynamic operation - 8

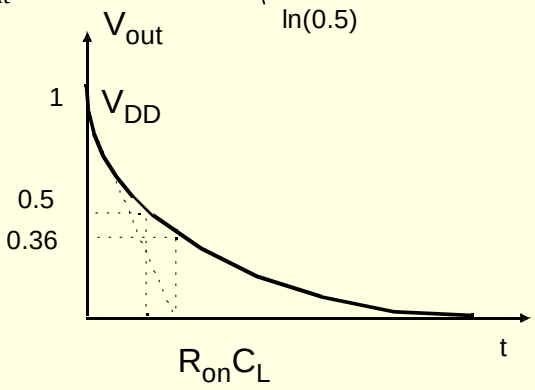
Propagation delay - 5



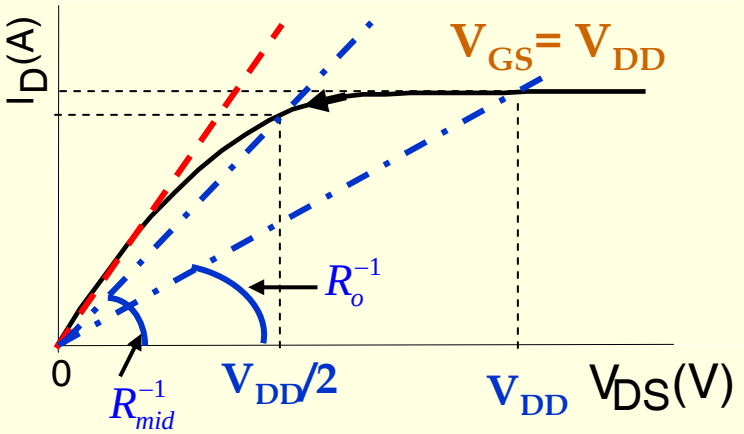
Approach 2

$$t_{pHL} = f(R_{on}.C_L) = 0.69\, R_{on}C_L$$

ln(0.5)



What's R_{on}?



Approach by Uyemura

$$R_{on}^{-1} = \left.\frac{dI_D}{dV_{DS}}\right|_{V_{DS}=0} = k_n\left(\frac{W}{L}\right)_n\left(V_{DD} - V_{Tn}\right)$$

Modeling capacitor discharge as in an RC circuit!

Approach by Rabaey

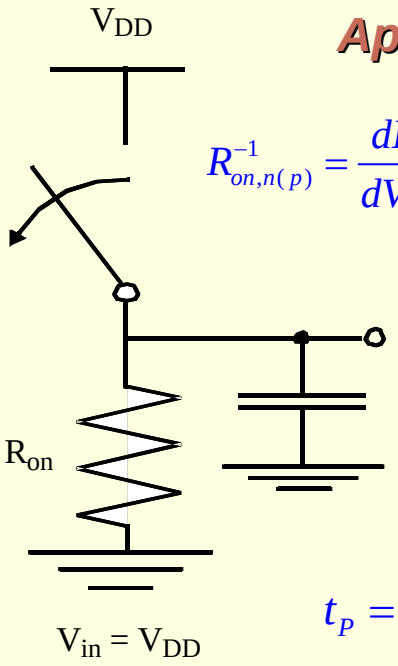
$$R_{on} \equiv \frac{1}{2}\left(R_0 + R_{mid}\right)$$

$$t_{PHL} \approx \frac{C}{k_n\left(\frac{W}{L}\right)_n V_{DD}}$$

Source: Rabaey

Dynamic operation - 9

Propagation delay - 6



Approach by Uyemura

$$R_{on,n(p)}^{-1} = \left.\frac{dI_D}{dV_{DS}}\right|_{V_{DS}=0} = k_{n(p)}\left(\frac{W}{L}\right)_{n(p)}\left(V_{DD} - (+)V_{Tn(p)}\right)$$

$$t_{pHL} = 0.69\, R_{on,n} C_L$$

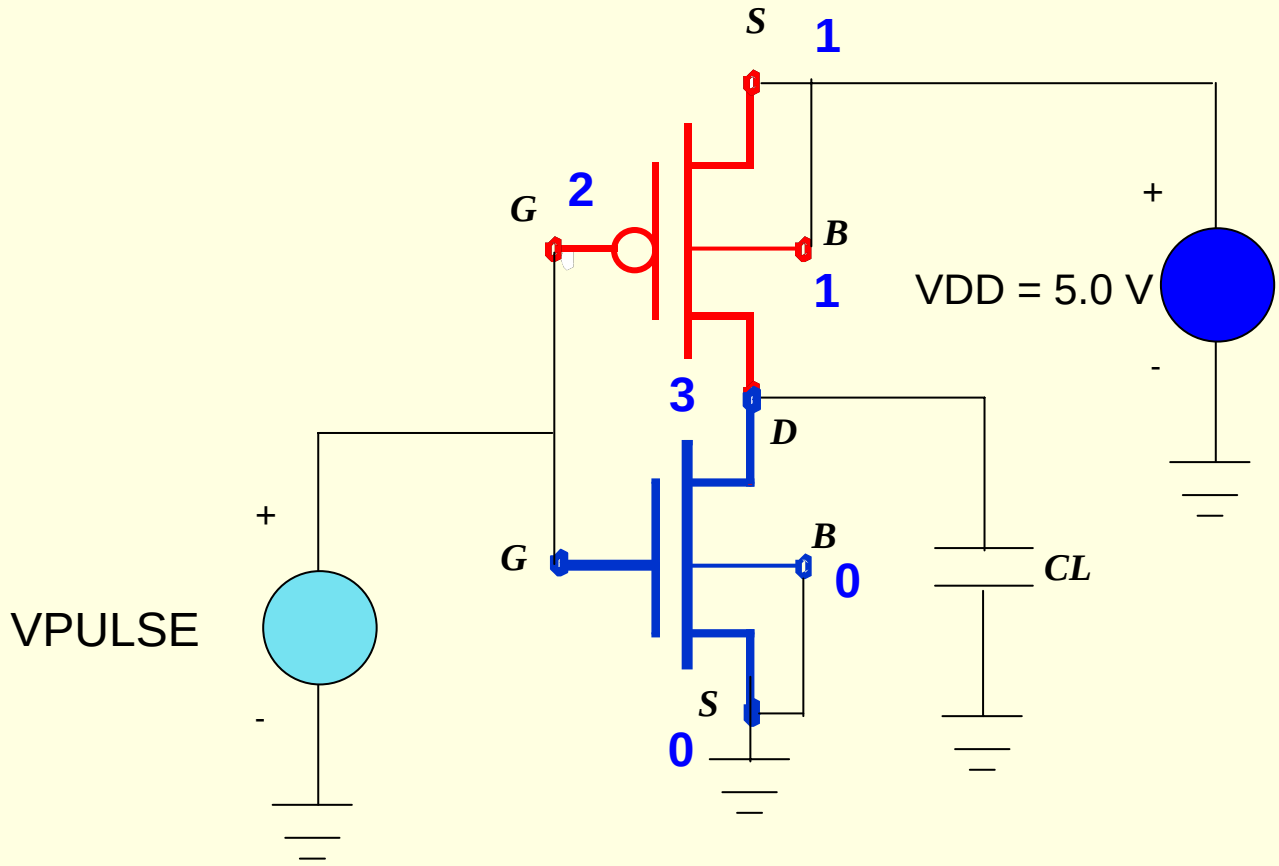
$$t_{pLH} = 0.69\, R_{on,p} C_L$$

$$t_P = \frac{t_{PHL} + t_{PLH}}{2} = \frac{0.69 \cdot C_L}{2}\left[\frac{1}{k_n\left(\frac{W}{L}\right)_n\left(V_{DD} - V_{Tn}\right)} + \frac{1}{k_p\left(\frac{W}{L}\right)_p\left(V_{DD} + V_{Tp}\right)}\right]$$

$$t_P \approx \frac{0.69 \cdot C_L}{2V_{DD}}\left[\frac{1}{k_n\left(\frac{W}{L}\right)_n} + \frac{1}{k_p\left(\frac{W}{L}\right)_p}\right]$$

Source: Uyemura

Dynamic operation - 10 Experimental setup



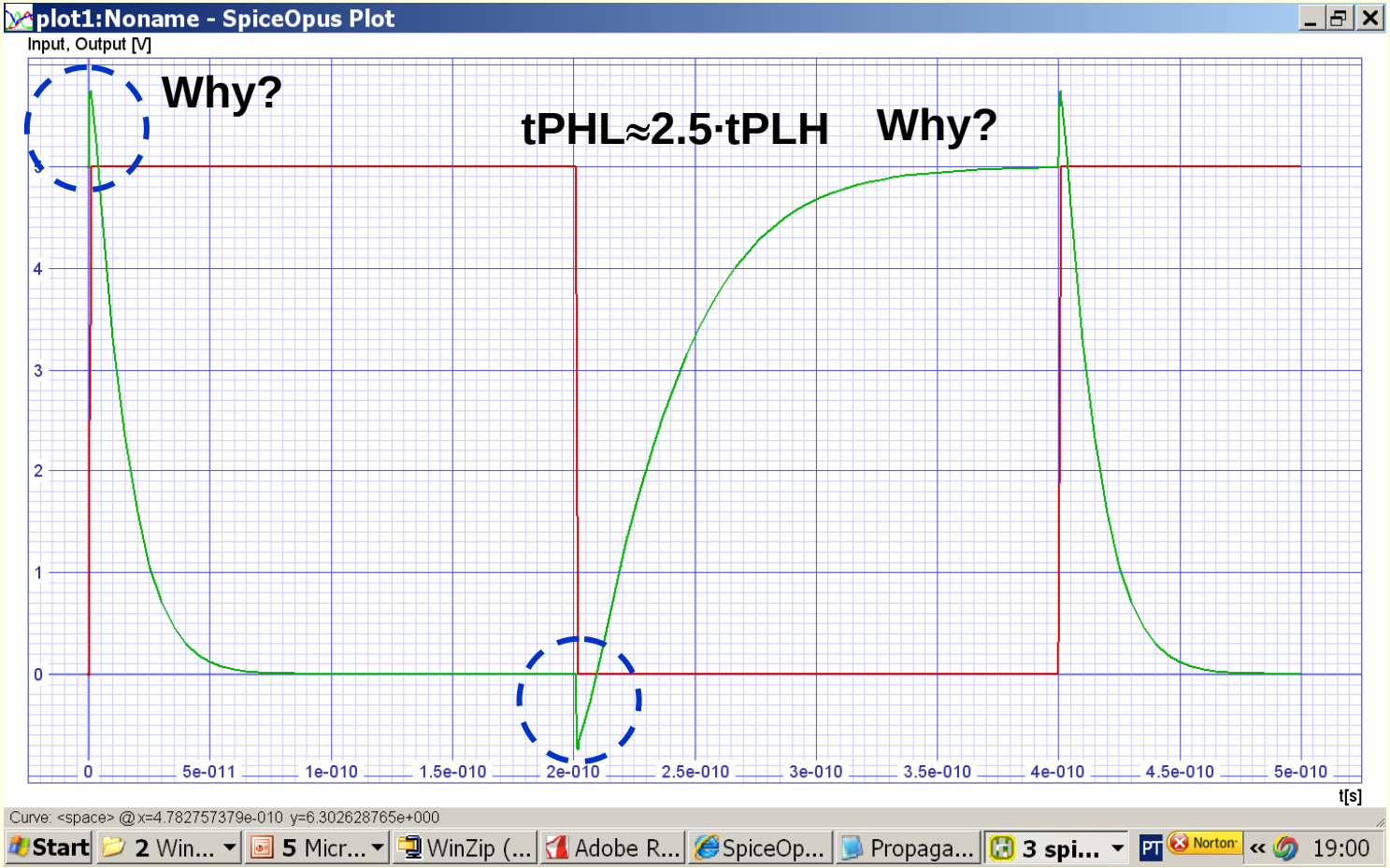
Dynamic operation - 11

```
Inverter Propagation Delay
* this is the Propagationdelay.cir file
* PMOS transistor description
MP 3 2 1 1 modelp W=2u L=1u
.model modelp pmos (level=1 VT0=-0.65 TOX=7.5n KP=60u lambda=0.0)
* NMOS transistor description
MN 3 2 0 0 modeln W=2u L=1u
.model modeln nmos (level=1 VT0=0.5 TOX=7.5n KP=150u lambda=0.0)
* dc source
vDD 1 0 dc 5.0
*load capacitance
CL 3 0 0.01p
*signal source
v0 2 0 dc 0 pulse 0 5 0 1ps 1ps 200ps 400ps
.end
```

Dynamic operation - 12

```
SpiceOpus (c) 6 -> source Propagationdelay1.cir
SpiceOpus (c) 7 -> tran 1ps 500ps
SpiceOpus (c) 8 -> setplot
            new      New plot
Current tran2        Inverter Propagation Delay  (Transient Analysis)
            tran1    Inverter Propagation Delay  (Transient Analysis)
            const    Constant values (constants)
SpiceOpus (c) 9 -> setplot tran2
SpiceOpus (c) 10 -> plot v(2) v(3) xlabel t[s] ylabel 'Input, Output [V]'
```

Dynamic operation - 12



Dynamic operation - 14

Exercise

Simulate the transient response of the inverter of the previous exercise for fan-outs of one and two inverters

Dynamic operation - 15

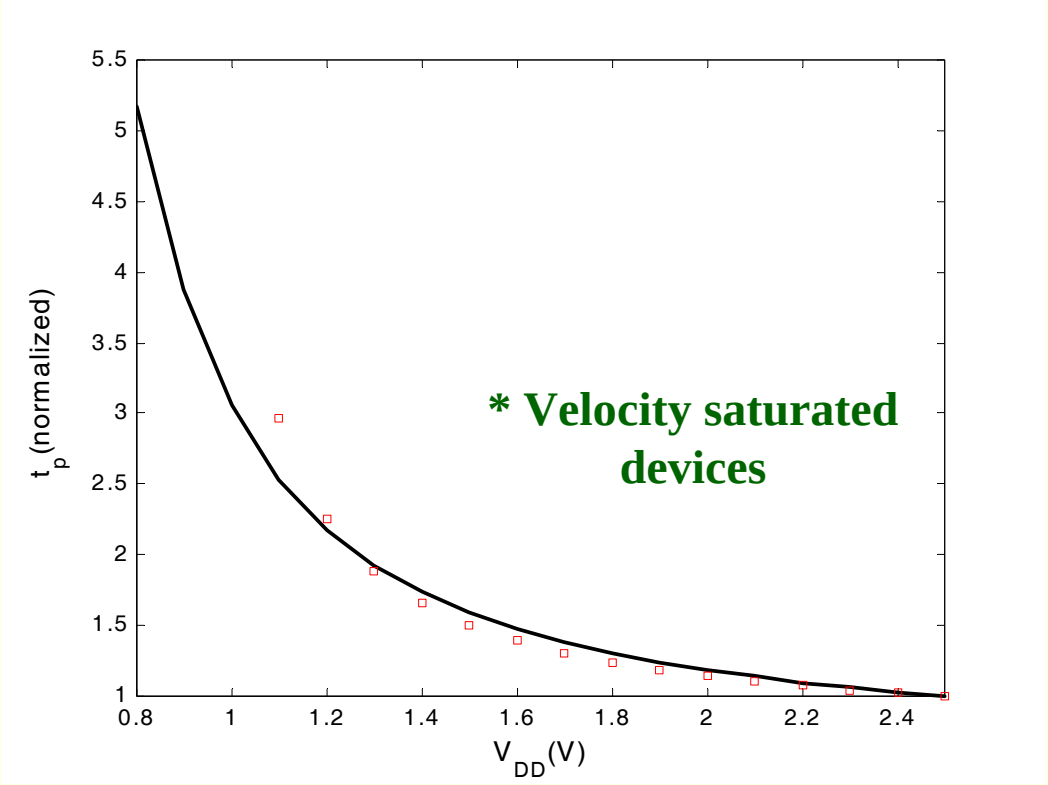
Design for Performance

- Keep capacitances small
- Increase transistor sizes (W)
  - watch out for self-loading!
- Increase VDD (????)

Dynamic operation - 16

Design for Performance

- Increase VDD (????)

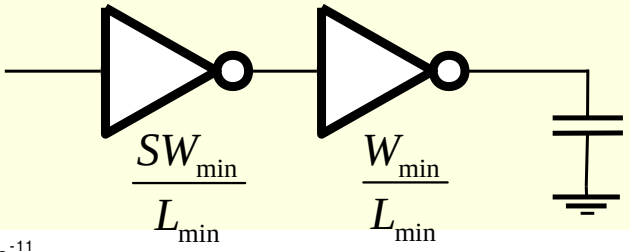


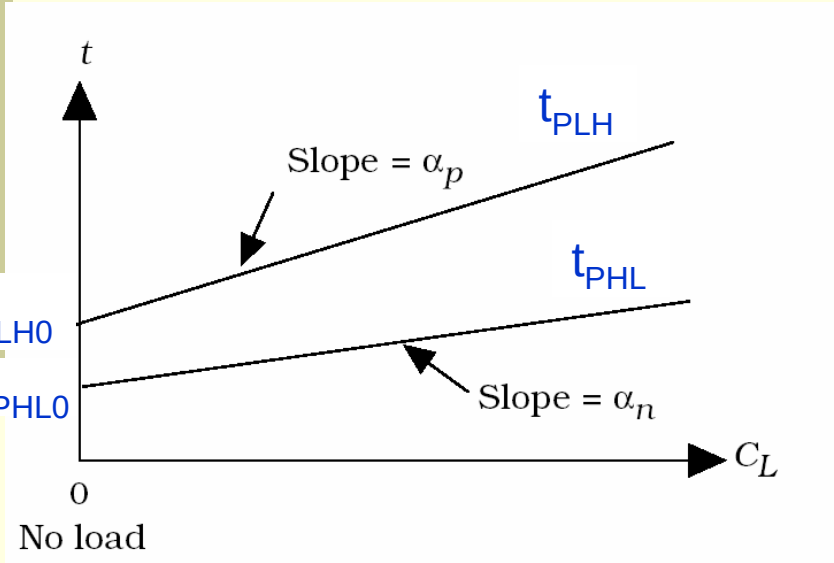
Source: Rabaey

Dynamic operation - 17

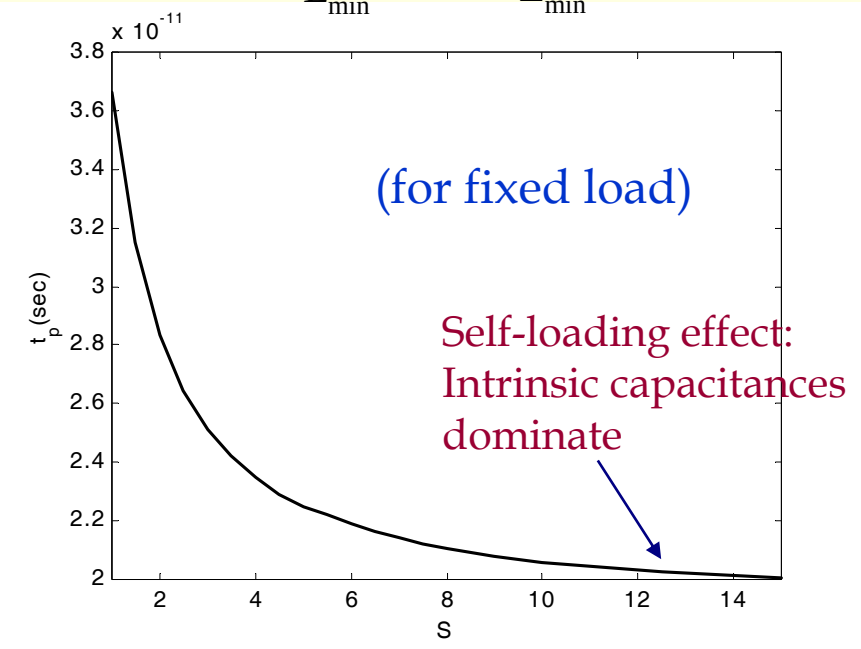
Design for Performance

- Increase transistor sizes (W)
  - watch out for self-loading





Propagation delays vs. load capacitance

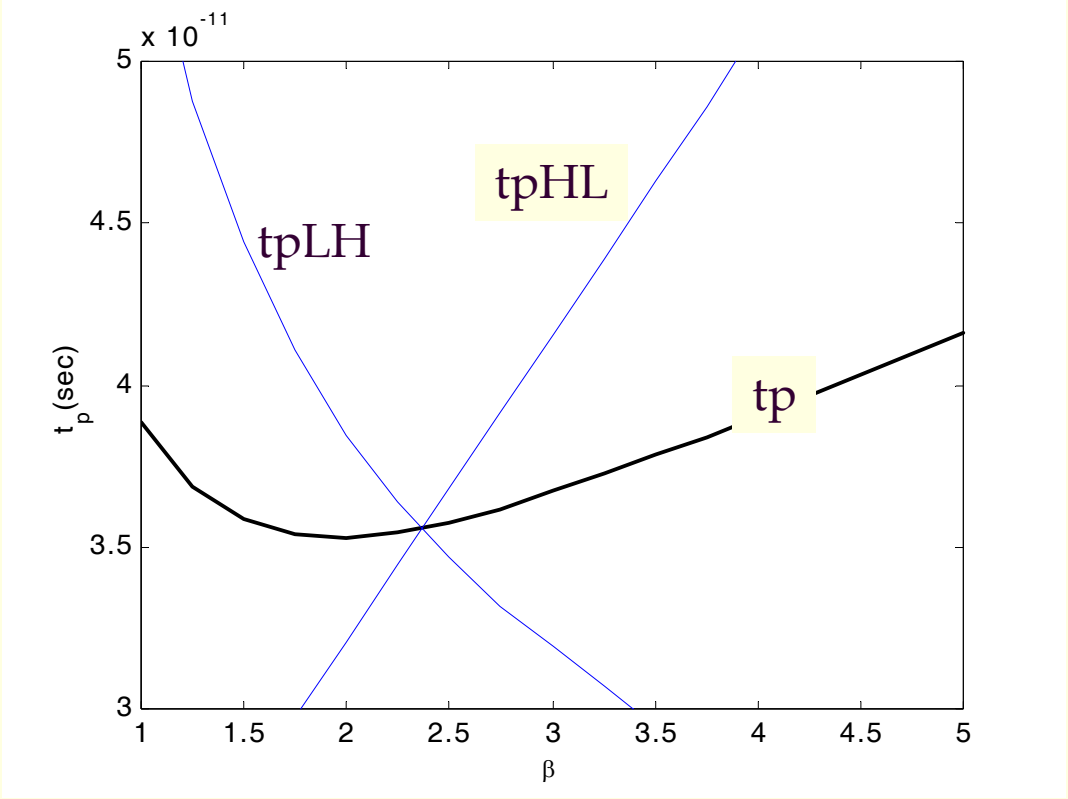


Source: Uyemura

Source: Rabaey

Dynamic operation - 18

Design for Performance

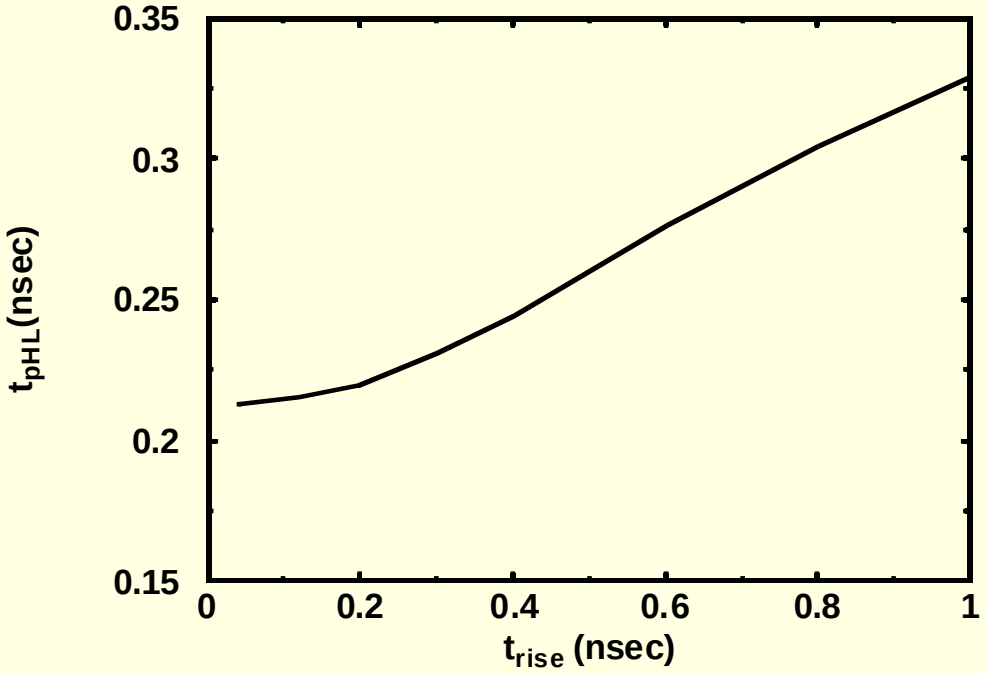


Propagation delays vs. PMOS-to-NMOS transistor ratio $\beta=W_p/W_n$

Source: Rabaey

Dynamic operation - 19

Impact of Rise Time on Delay



$$t_{pHL} = \sqrt{t_{pHL(step)}^2 + (t_r/2)^2}$$

Source: Rabaey