Digital Integrated Circuits

Chapter 6 – The CMOS Inverter

Contents

- Introduction (MOST models) 0, 1st, 2nd order
- The CMOS inverter : The static behavior:
  - DC transfer characteristics,
  - Short-circuit current
- The CMOS inverter : The dynamic behavior
- Energy, power, and energy delay

Introduction - 1

Zero-order model (ideal switch)
of n- and p-channel MOSFETs

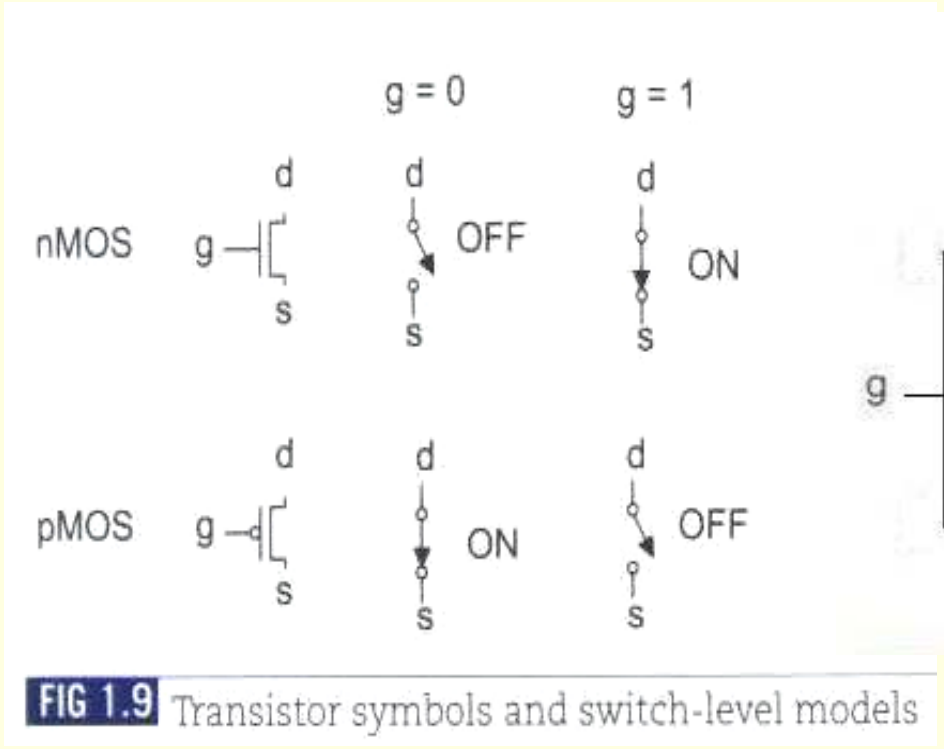
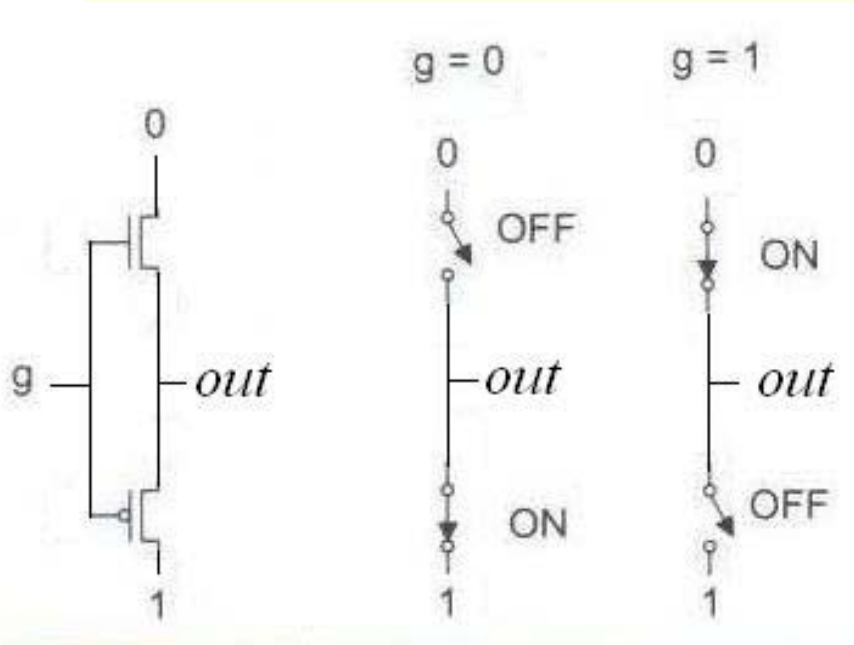


FIG 1.9 Transistor symbols and switch-level models



Inverter

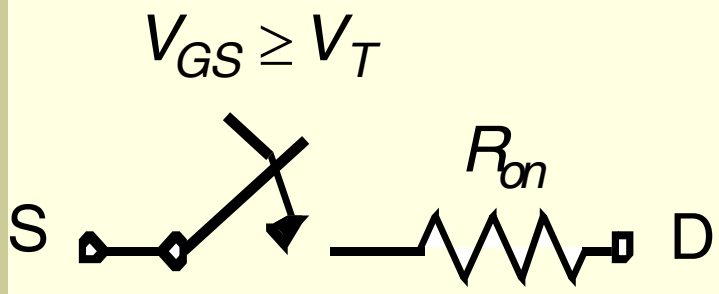
What for a signal between “0” and “1”?

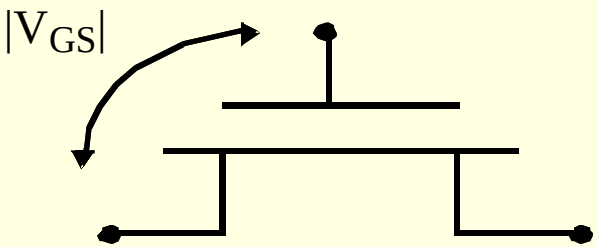
Source: Weste & Harris

Introduction - 2

First-order model of a MOSFET

Non ideal switch ⟷ An MOS Transistor



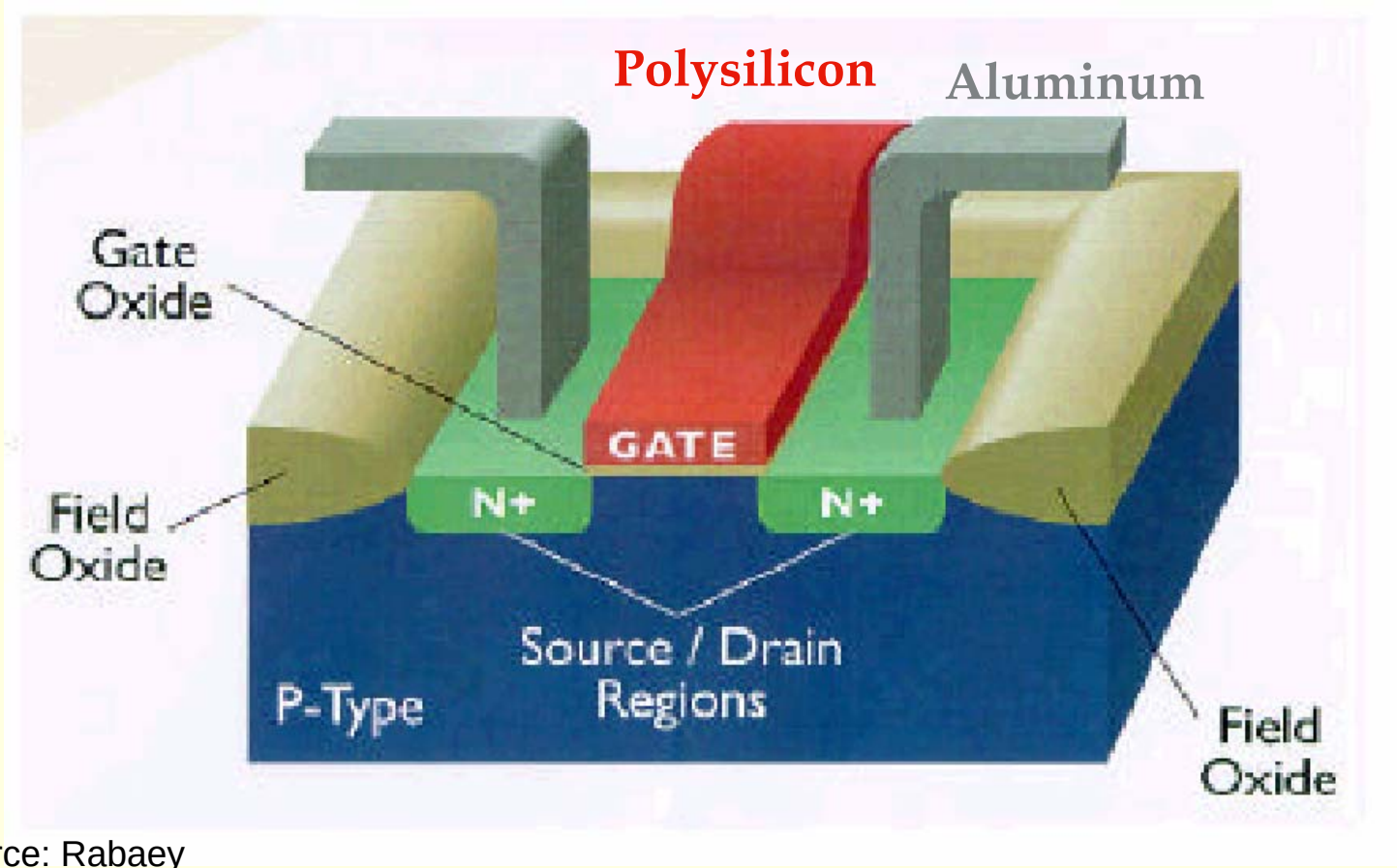


What's the value of R_{on}? Abrupt transition from on to off?

Source: Rabaey

Introduction - 3

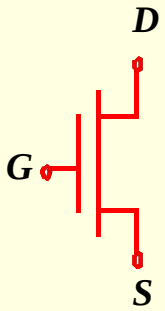
The MOS Transistor

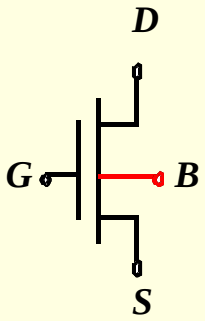


Source: Rabaey

Introduction - 4

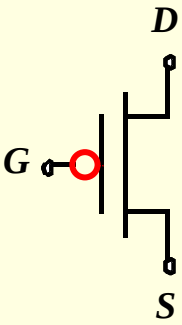
MOS Transistors – n- and p-channel

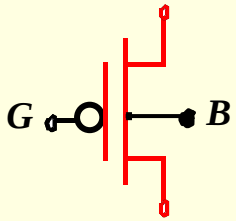




In general connected to GND

NMOS Enhancement



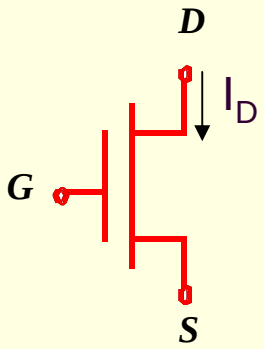


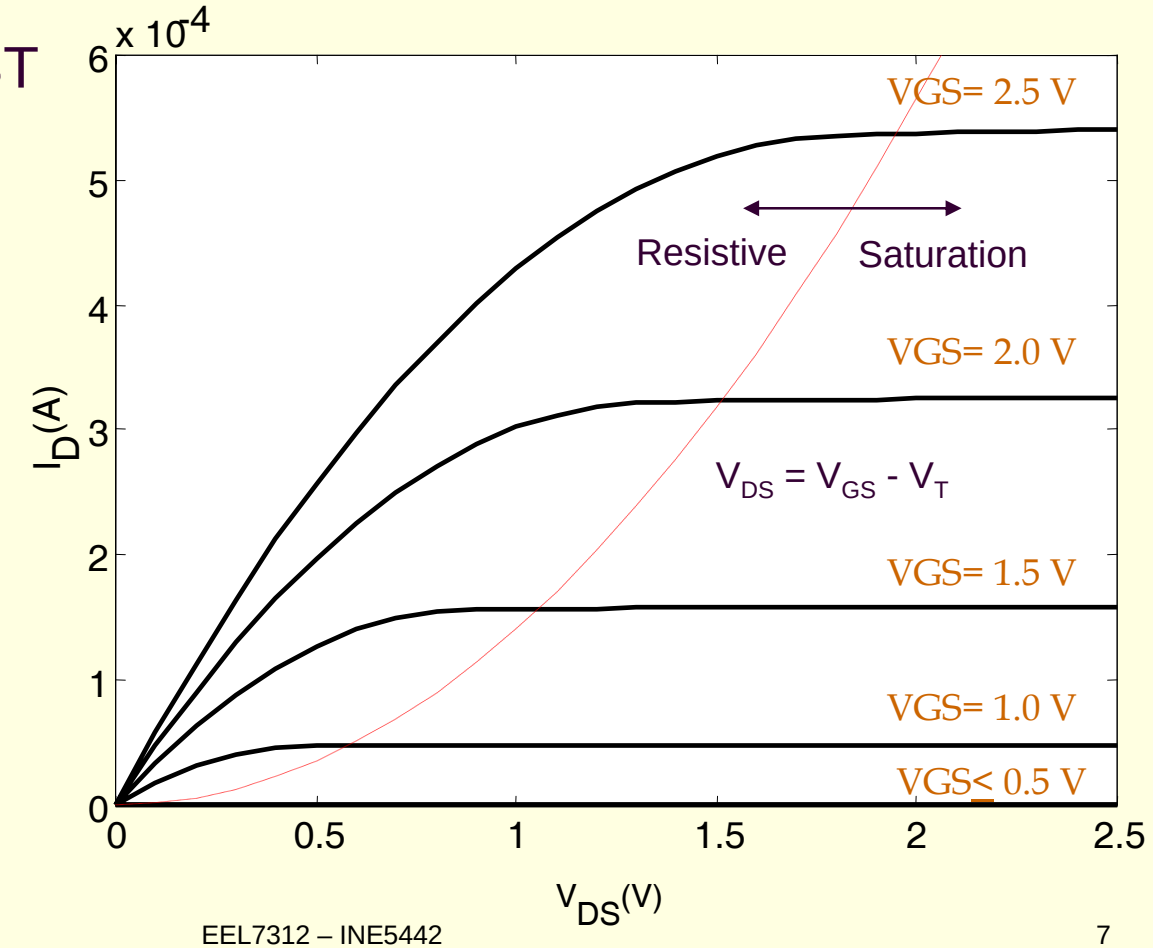
In general connected to V_{DD}

PMOS Enhancement

Introduction - 5

I-V Relations
Long-channel n-MOST

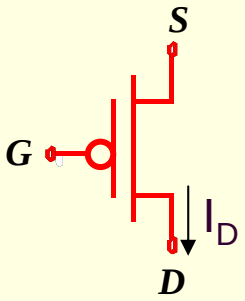


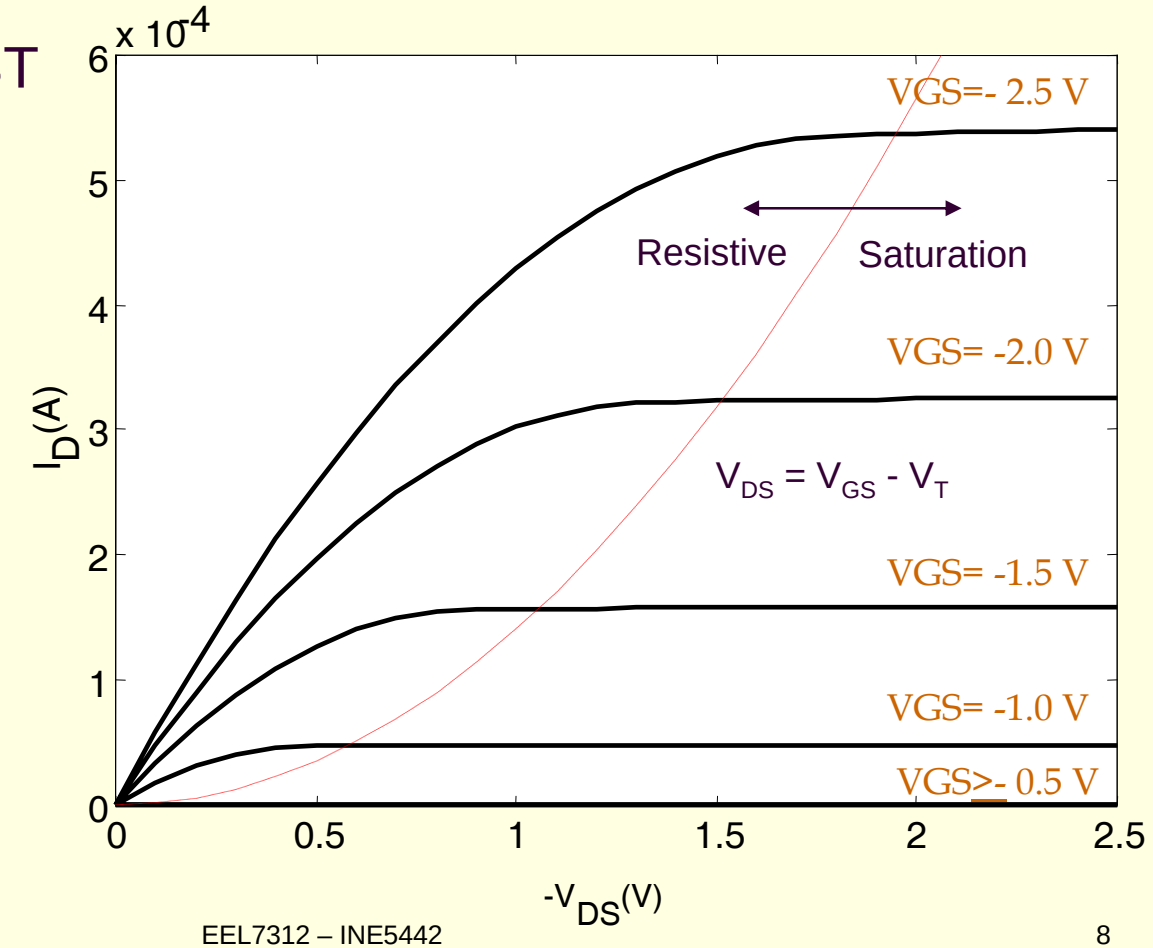


Source: Rabaey

Introduction - 6

I-V Relations
Long-channel p-MOST





Source: Rabaey

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Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)(1 + \lambda V_{DS})$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$

Process Transconductance Parameter

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

Channel Length Modulation

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

Introduction - 8

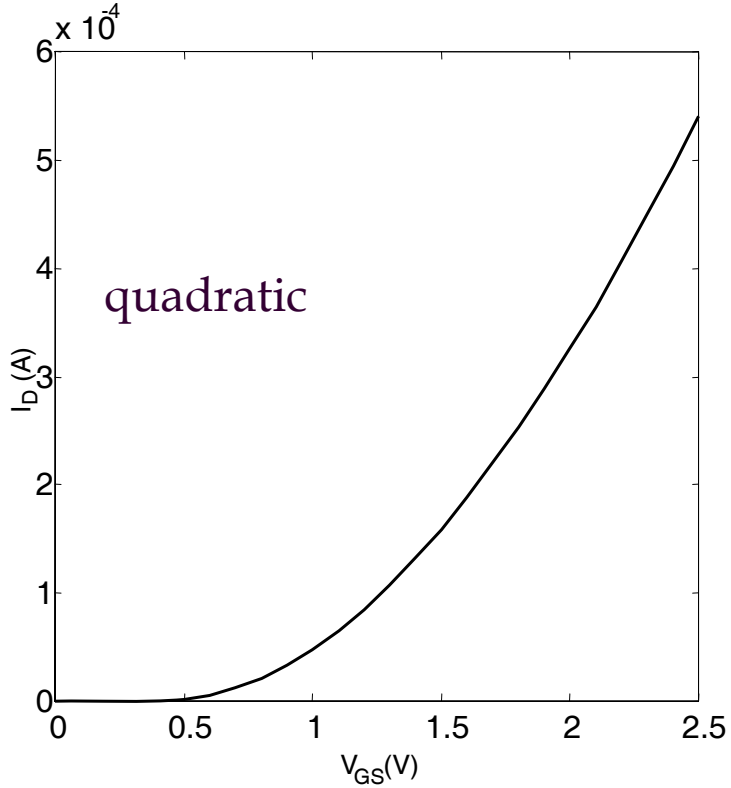
I_D versus V_{GS}

Saturation mode: $V_{DS} > V_{GS} - V_T$

V_{DS}=2.5 V V_T = 0.5 V

constant

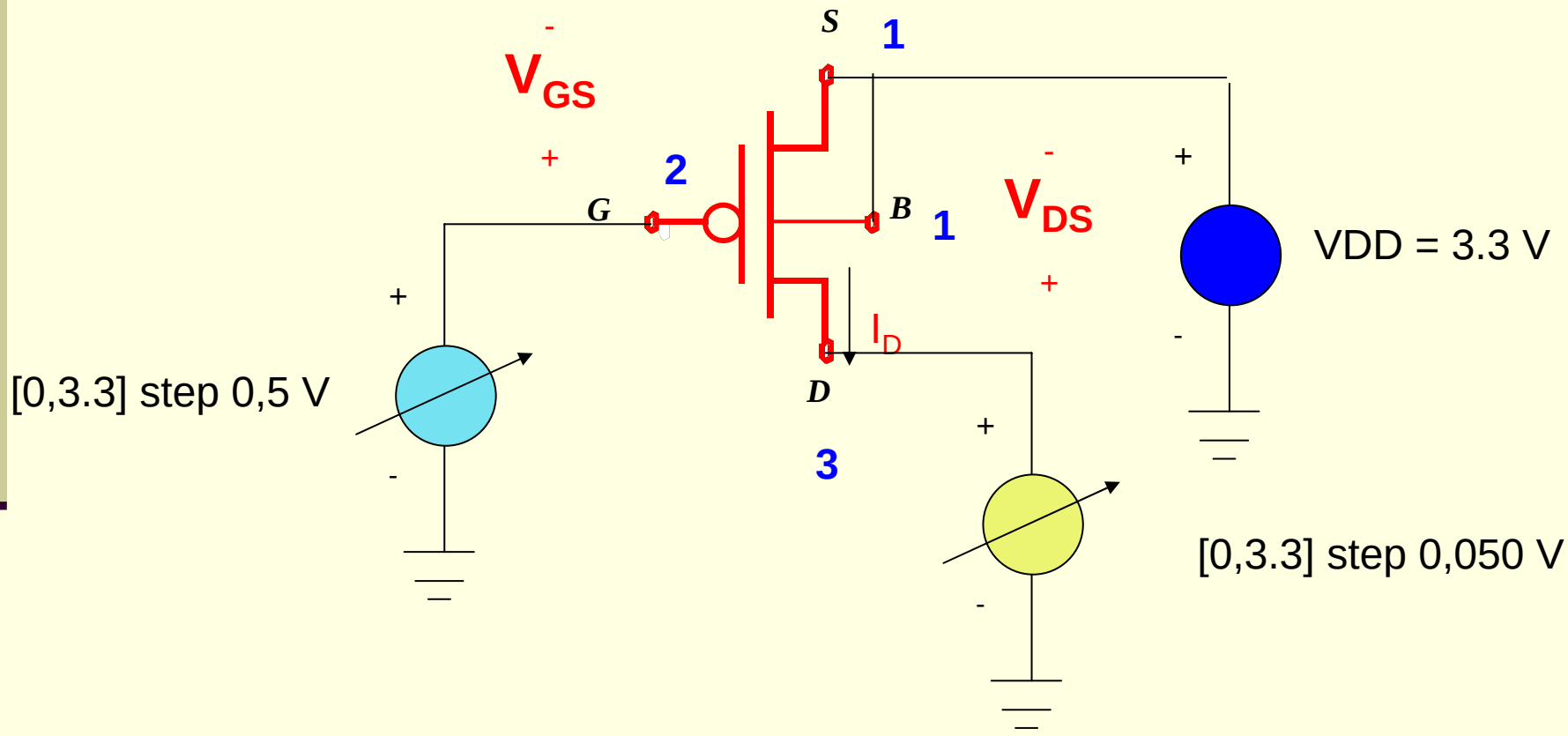
$$I_D = \frac{k'_n W}{2 L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$



Source: Rabaey

Introduction – 9

Experimental setup

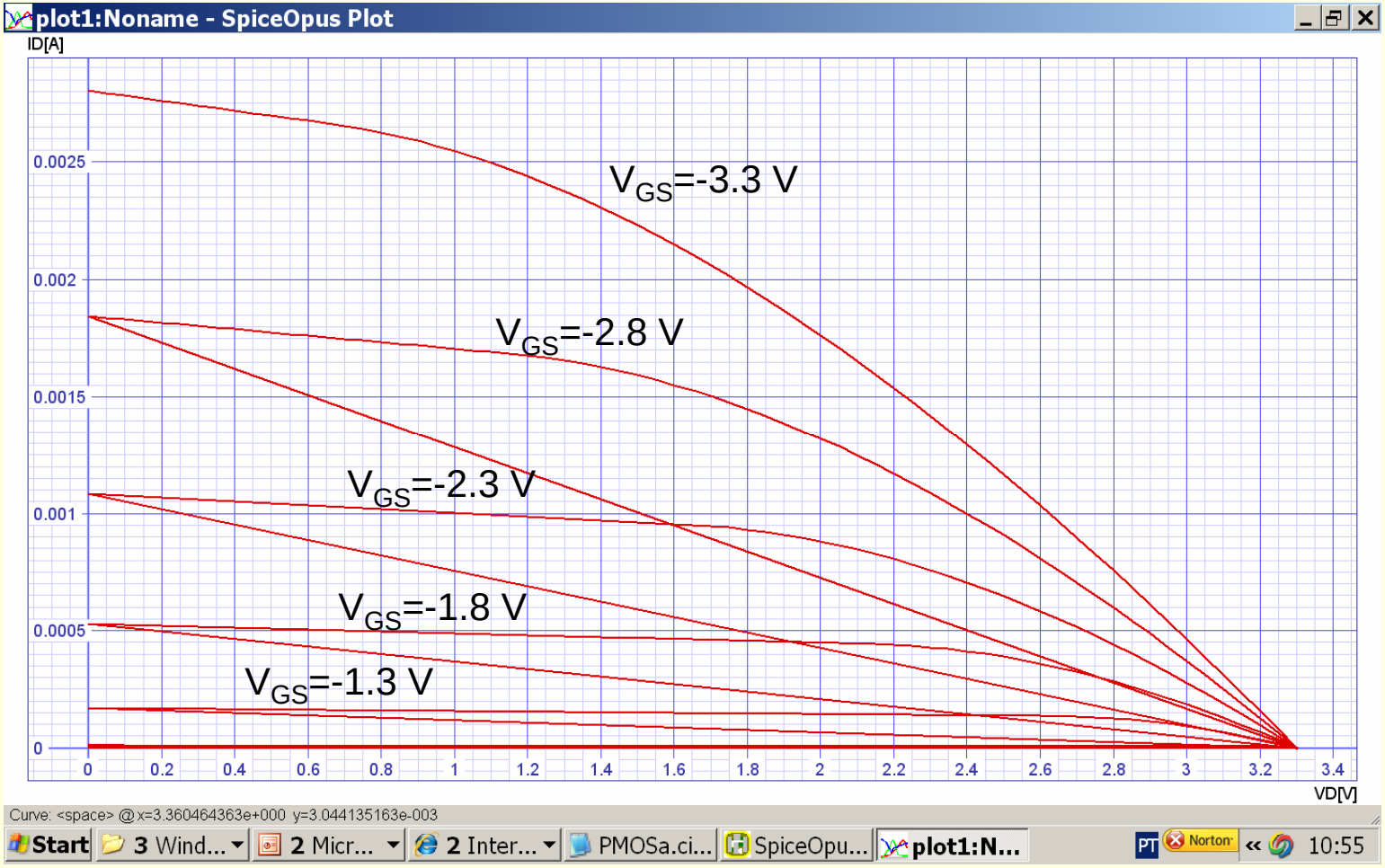


Introduction – 9 An experiment

- Circuit description (SPICE)
  - http://www.inf.ufsc.br/~santos/ine5442/experiment/PMOSa.cir
- Steps
  - http://www.inf.ufsc.br/~santos/ine5442/experiment/roteiro.txt

Introduction – 10

Simulation 6.1a
lambda = 0.1



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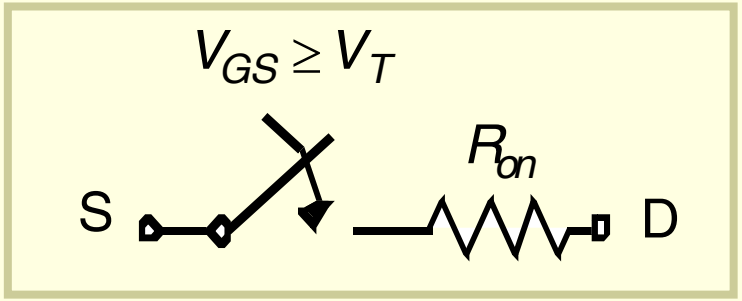
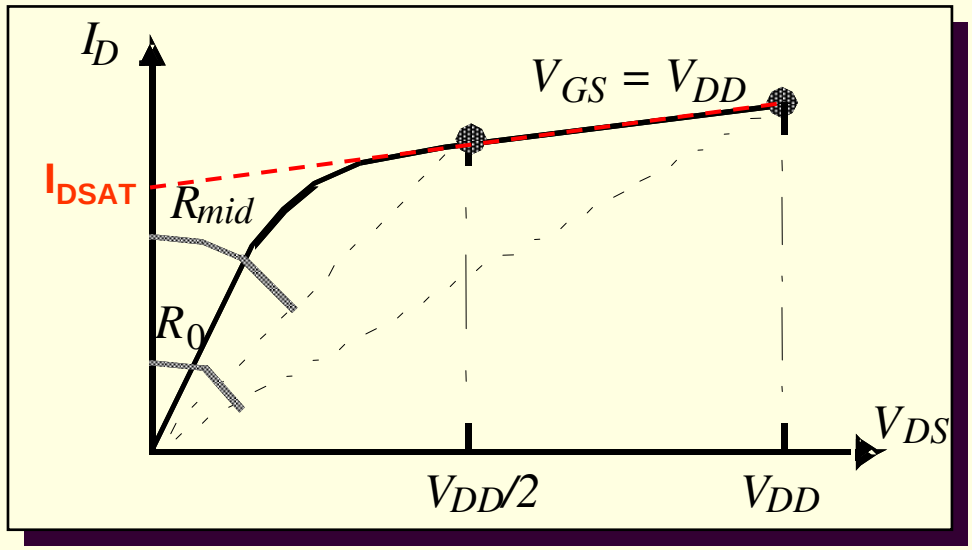
The Transistor as a Switch





$$R_{eq} \equiv \frac{1}{2}\left(R_0 + R_{mid}\right)$$

$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)$$

$$I_{DSAT} \equiv \frac{K_P}{2}\frac{W}{L}\left(V_{DD} - V_T\right)^2$$

Source: Rabaey

Introduction - 13

CMOS static logic – the beginning

WEDNESDAY, FEBRUARY 20, 1963 . . . UNIVERSITY OF PENNSYLVANIA—IRVINE AUDITORIUM . . . 2:50-5:30 P.M.

SESSION III: Logic I

WPM 3.5: Nanowatt Logic Using Field-Effect Metal-Oxide Semiconductor Triodes

F. M. Wanlass and C. T. Sah

Fairchild Semiconductor Div., Fairchild Camera-Instrument Corporation

Palo Alto, Calif.

32 • 1963 International Solid-State Circuits Conference

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CMOS static logic – the beginning

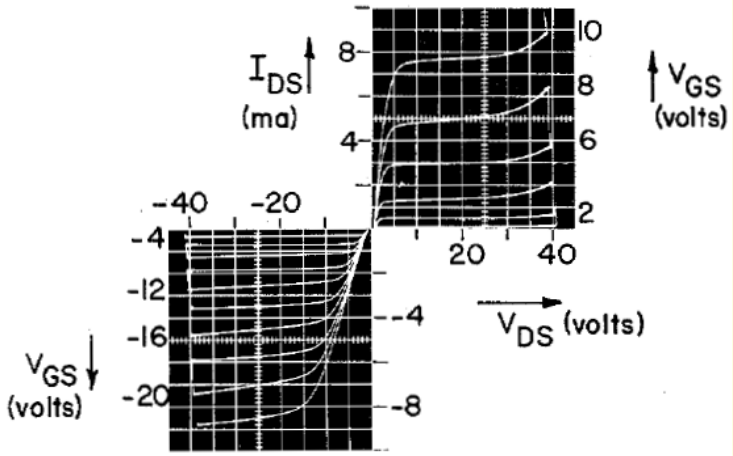

FIGURE 3—Characteristic curves for the field-effect triodes where drain current is plotted against drain voltage for source grounded and for different values of gate bias. The *N* element curves are plotted in the first quadrant.

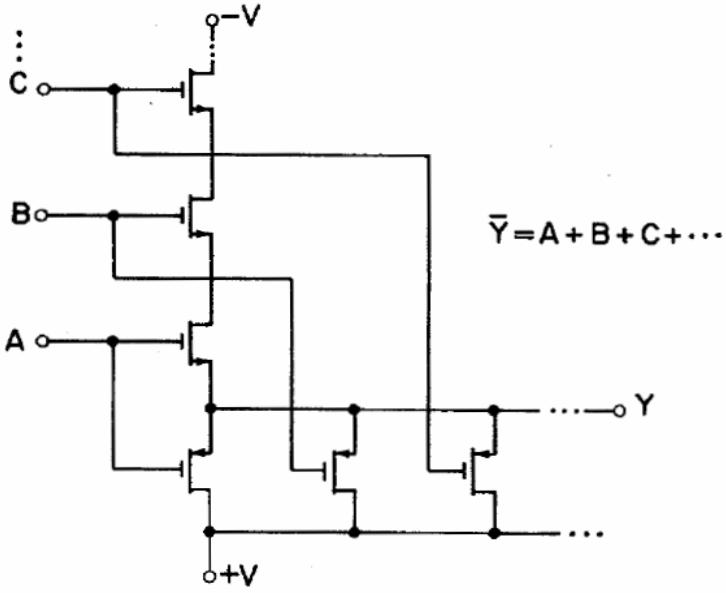

FIGURE 7—*NOR* logic circuit. If any of the inputs are + *V* then the output will be — *V*.

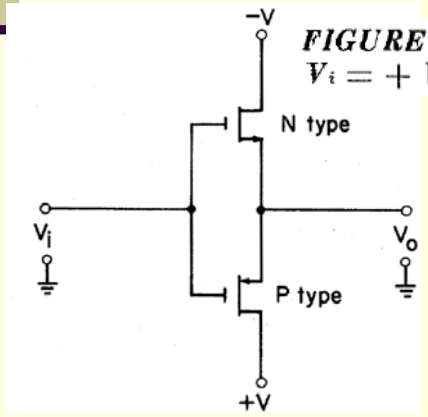

FIGURE 4—Low standby power inverter circuit; when $V_i = +V$, $V_o = -V$ and when $V_i = -V$, $V_o = +V$.

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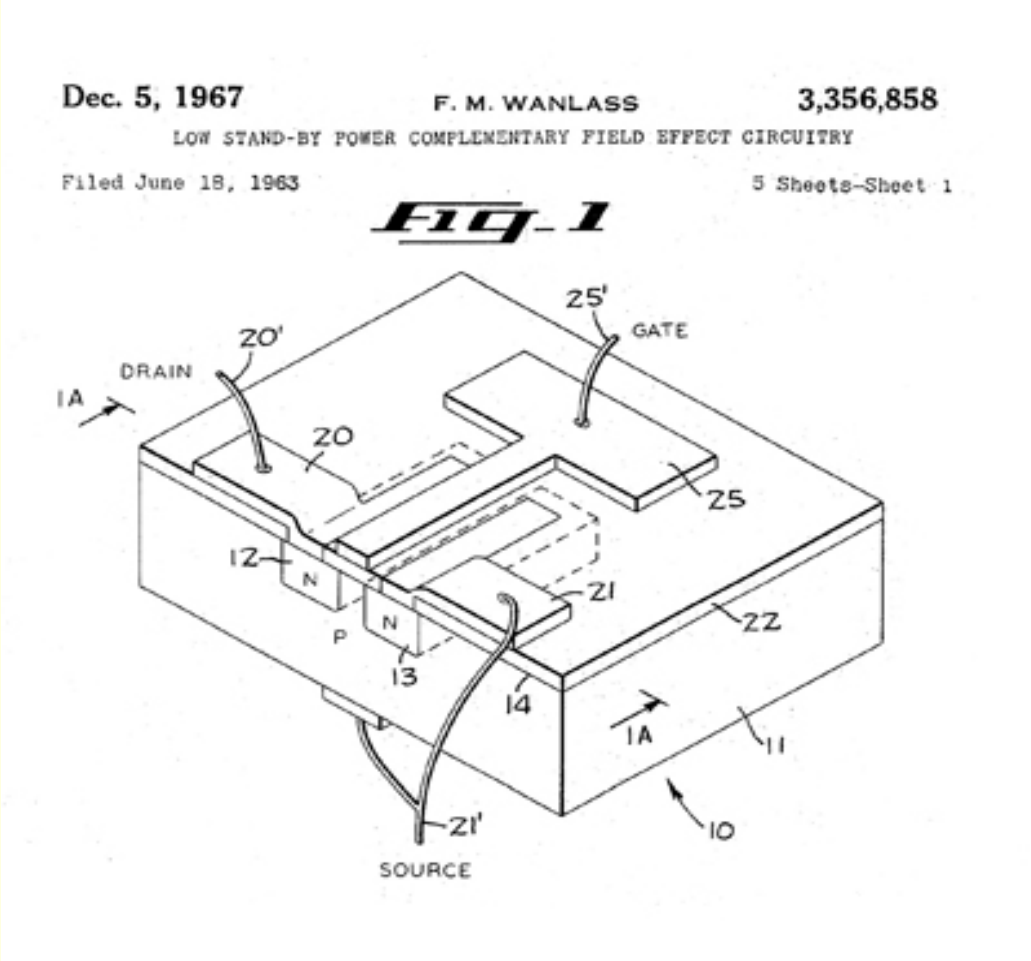
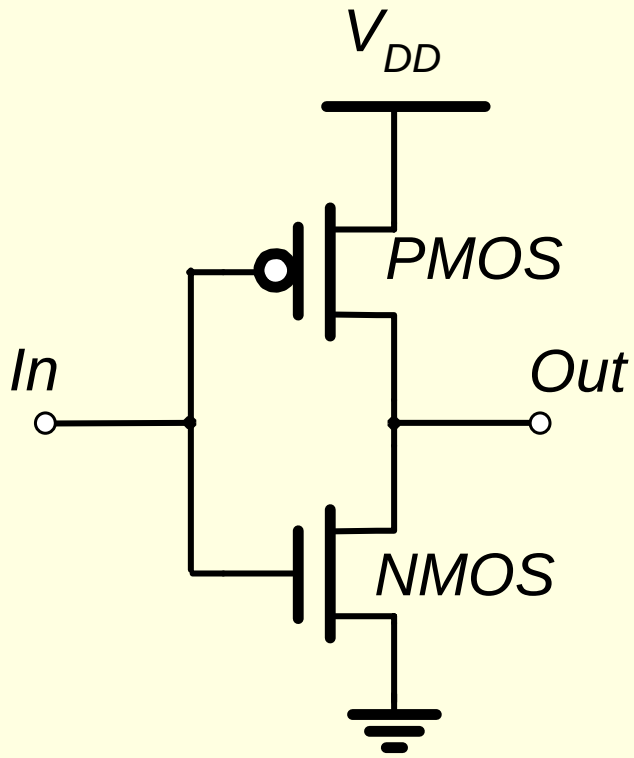
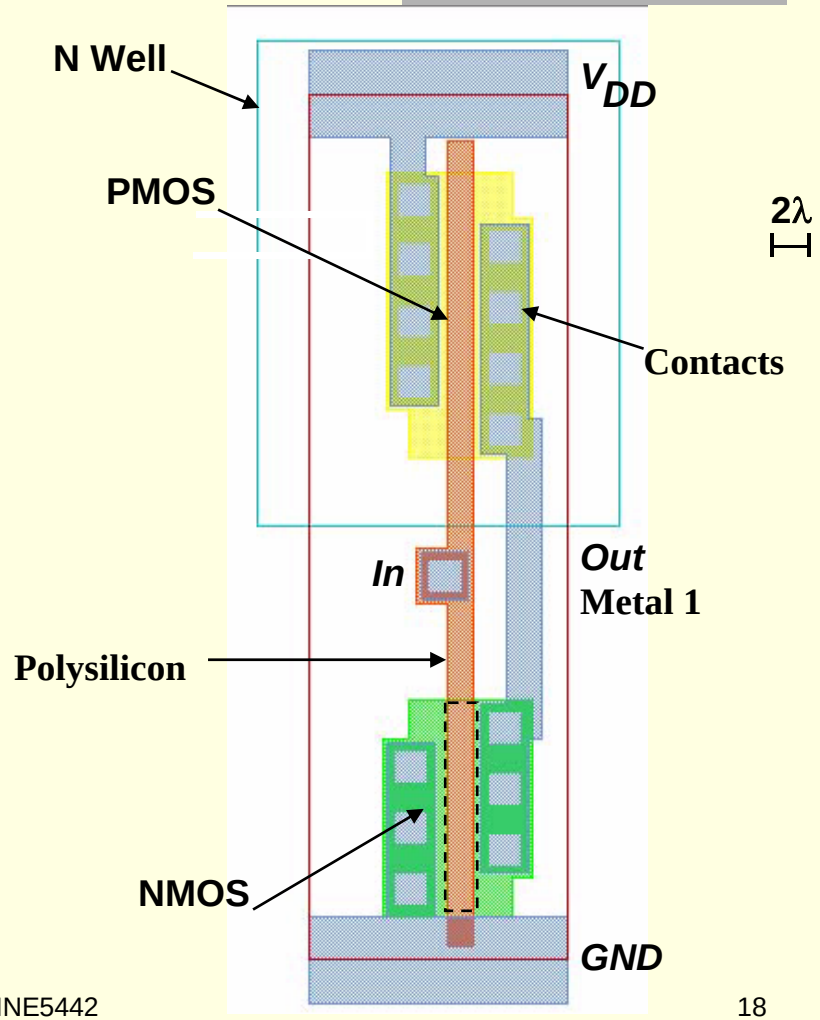
COMPUTER HISTORY MUSEUM

CMOS device structure from Frank Wanlass's patent drawing.
U. S. Patent Office.



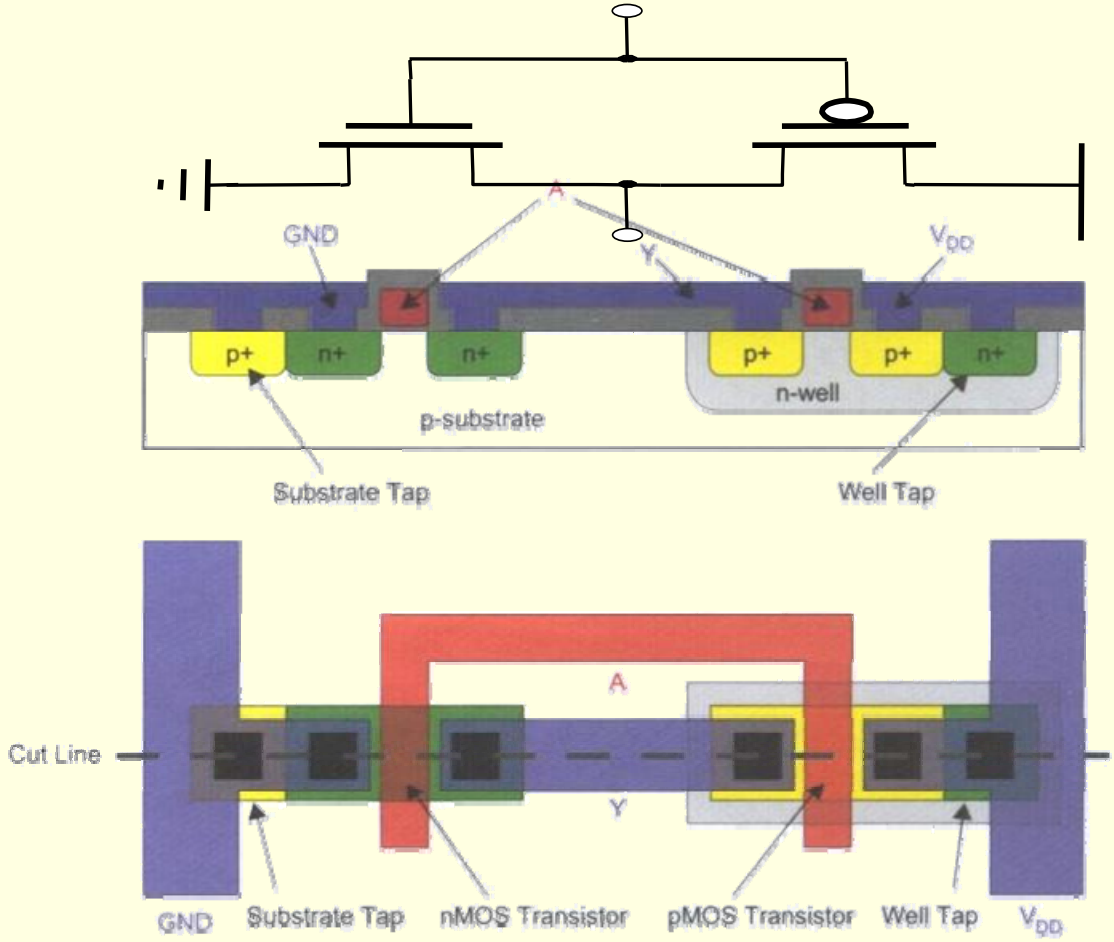
Introduction - 16 Schematic and layout -1





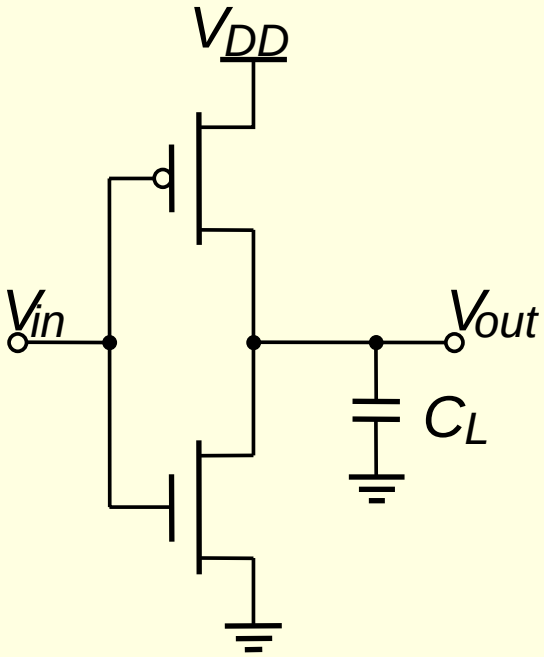
Source: Rabaey

Introduction - 17 Schematic and layout -2

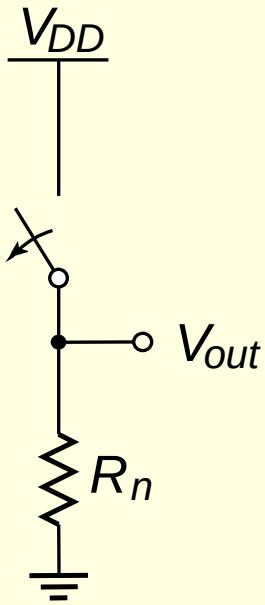


Figs 1.34–1.35(a) Inverter Cross-Section and Top View

Static characteristics - 1



V_{in}	0	V_{DD}
NMOS	OFF	ON
PMOS	ON	OFF
V_{out}	V_{DD}	0



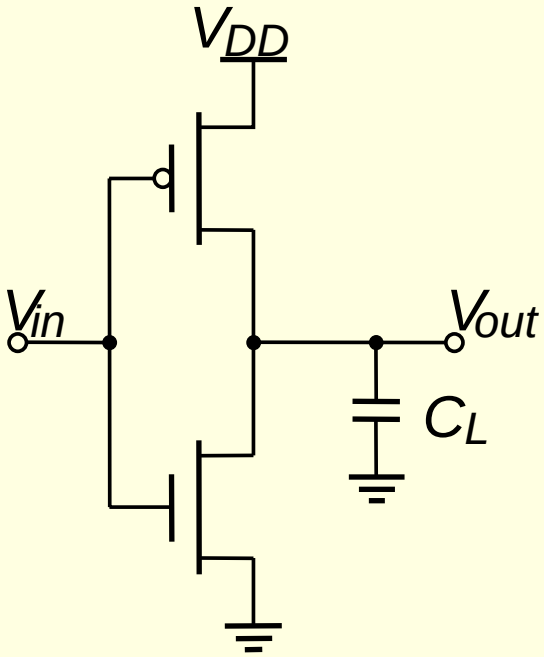
$V_{in} = V_{DD}$

$V_{GSn} = V_{DD} > V_{Tn}$

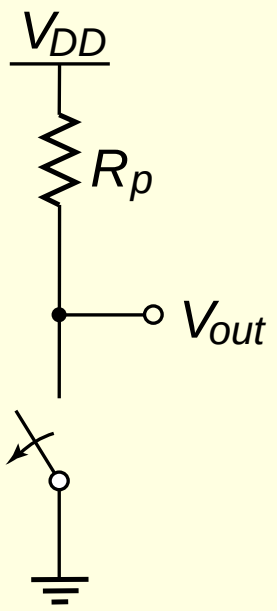
$V_{GSp} = 0 > V_{Tp}$

Source: Rabaey

Static characteristics - 1



V_{in}	0	V_{DD}
NMOS	OFF	ON
PMOS	ON	OFF
V_{out}	V_{DD}	0



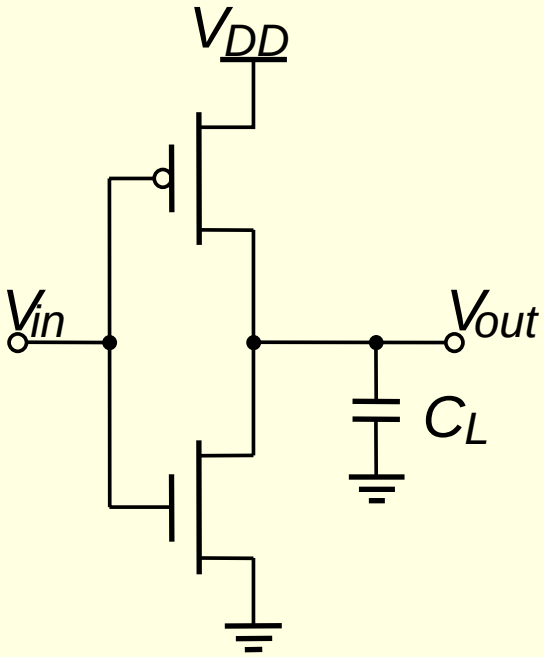
$V_{in} = 0$

$V_{GSn} = 0 < V_{Tn}$

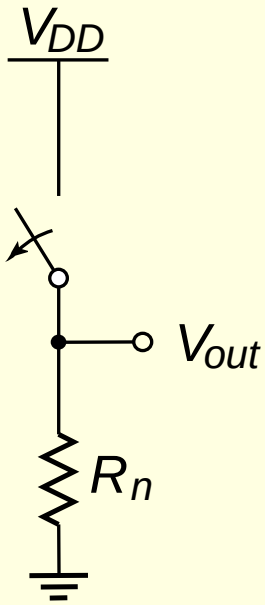
$V_{GSp} = -V_{DD} < V_{Tp}$

Source: Rabaey

Static characteristics - 1



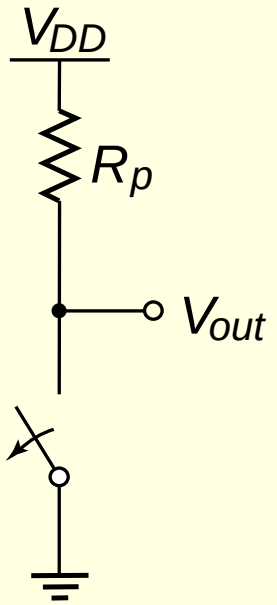
V_{in}	0	V_{DD}
NMOS	OFF	ON
PMOS	ON	OFF
V_{out}	V_{DD}	0



$V_{in} = V_{DD}$

$V_{GSn} = V_{DD} > V_{Tn}$

$V_{GSp} = 0 > V_{Tp}$



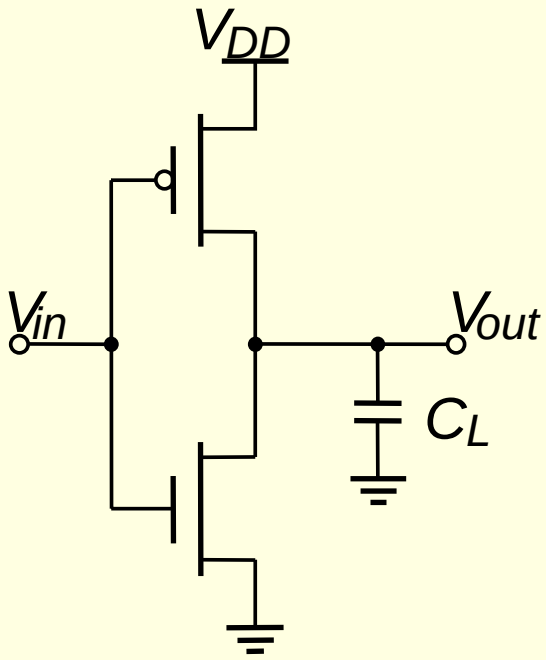
$V_{in} = 0$

$V_{GSn} = 0 < V_{Tn}$

$V_{GSp} = -V_{DD} < V_{Tp}$

Source: Rabaey

Static characteristics - 2



Voltage swing is equal to the supply voltage;

Logic levels are not dependent upon the relative device sizes;

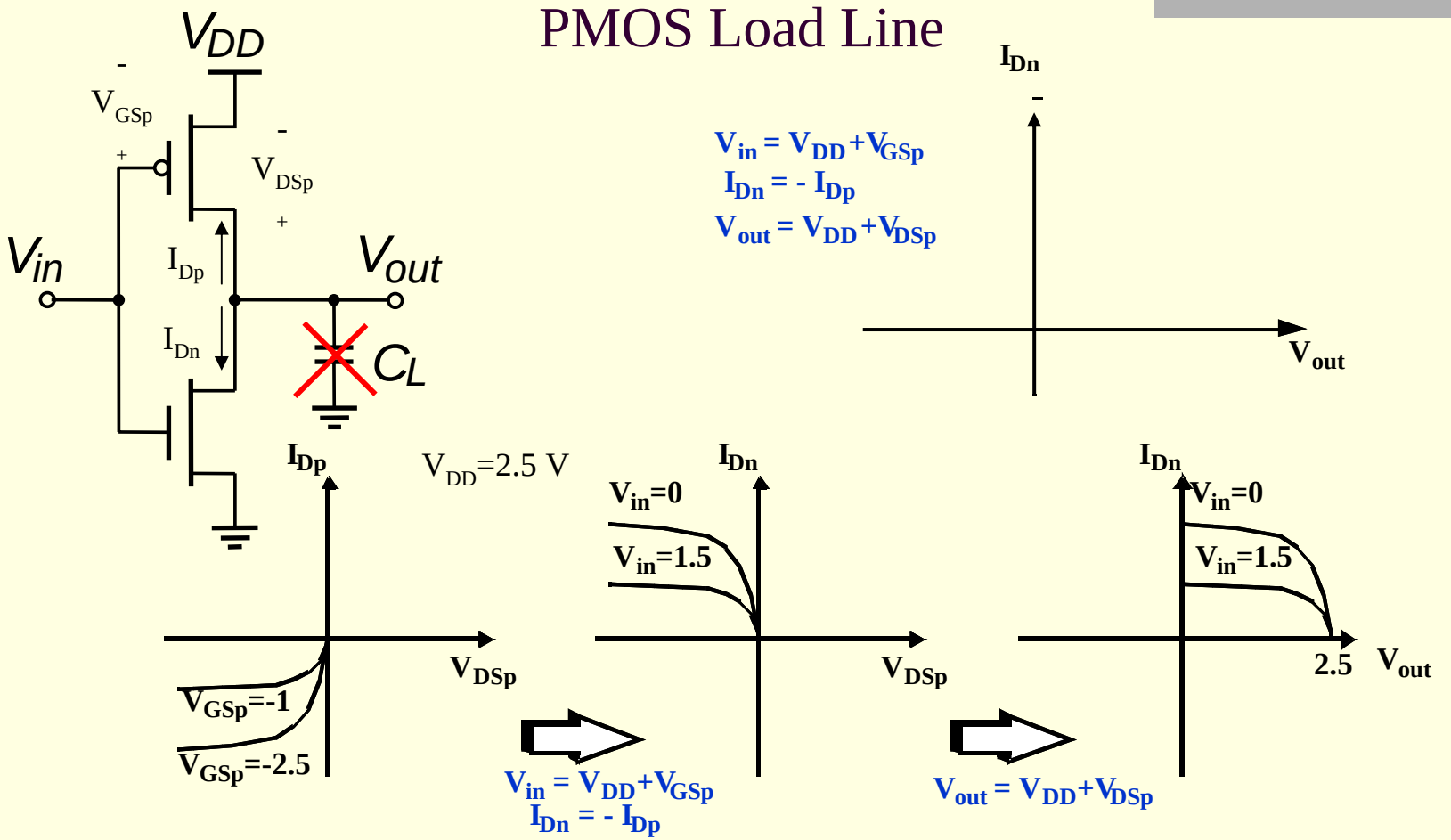
In steady state there always exists a path with finite resistance between the output and either V_{DD} or ground;

The input resistance $\rightarrow\infty$;

No direct path exists between supply and ground rails under steady-state operating conditions (this is first order approx. and is far from reality in more advanced technologies) $\rightarrow$ static power ≈ 0

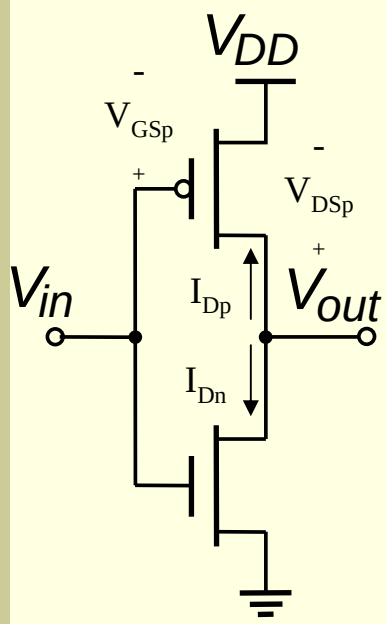
Source: Rabaey

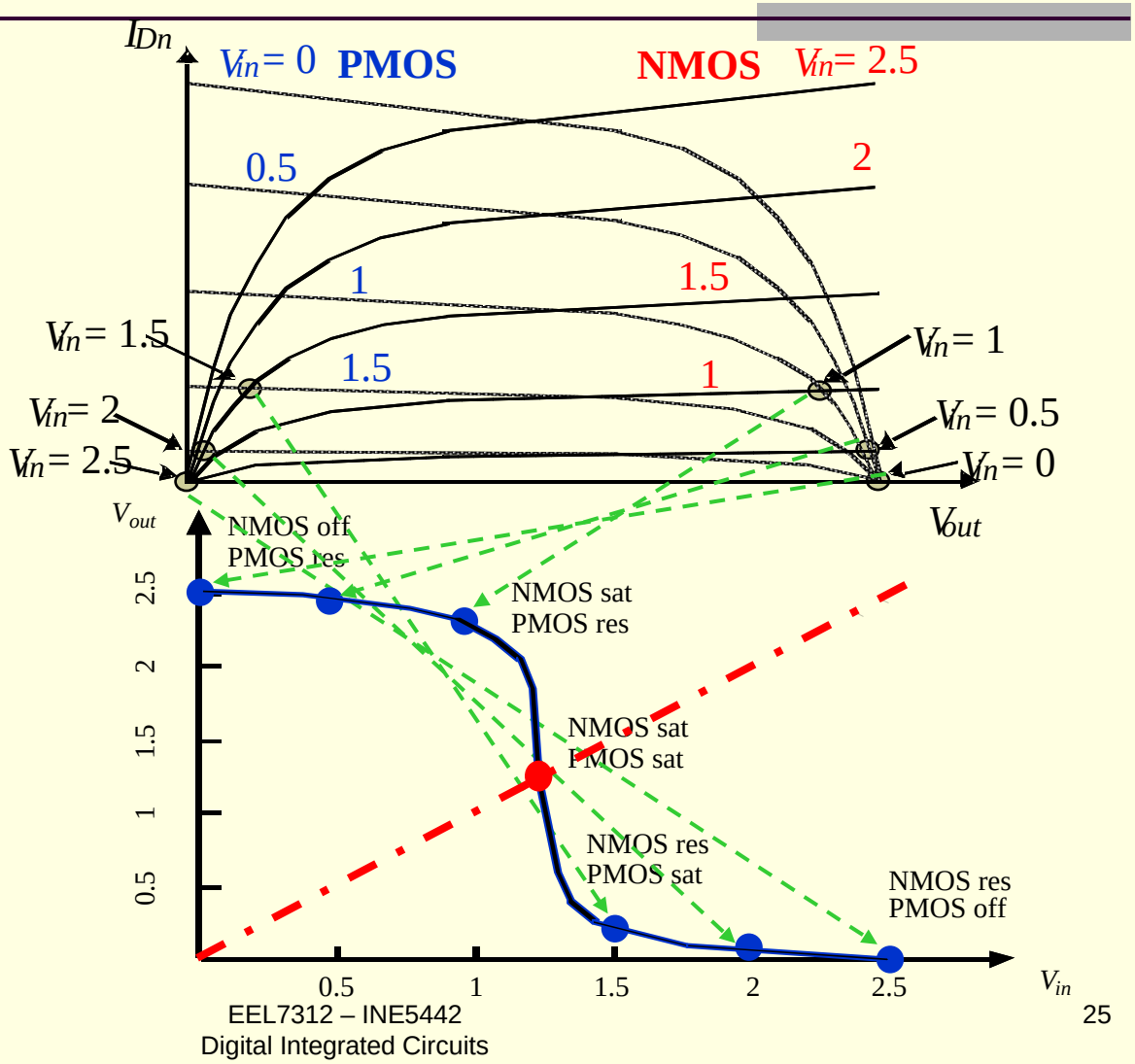
Static characteristics - 3



Source: Rabaey

Static characteristics - 4 VTC





Source: Rabaey