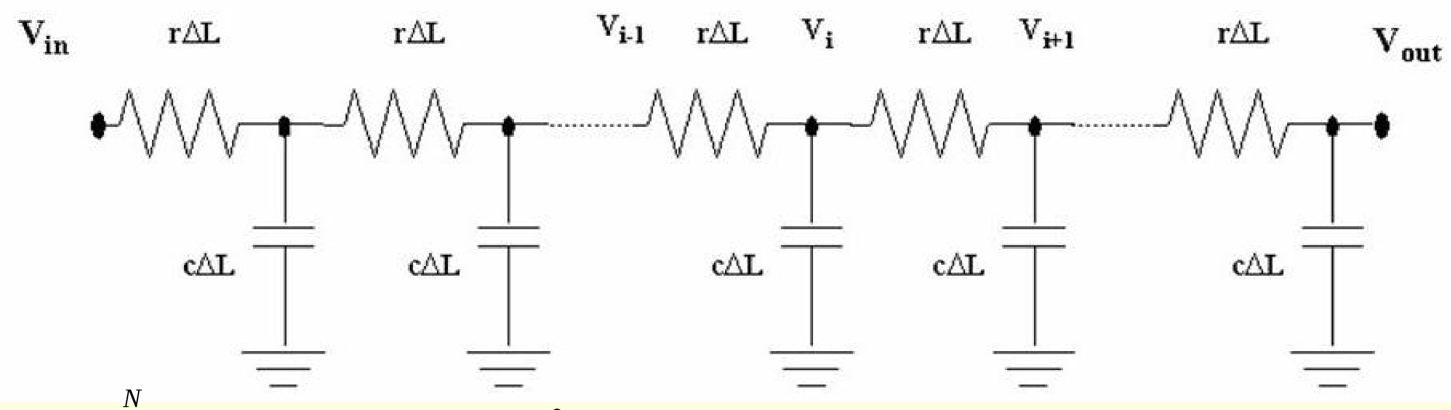
RC delay – 4: The Elmore delay - 3

Application of the Elmore delay formula to a (RC) wire.

Let R, C, and l be the total line resistance, capacitance, and length.

$r = R/l; \quad c = C/l; \quad \Delta L = l/N$



$$\tau_{Dout} = \sum_{i=1}^{N} (ir\Delta L)c\Delta L = rc(\Delta L)^2 (1+2+....+N) =$$

$$rc(l/N)^2 \frac{1+N}{2} N = rcl^2 \frac{1+N}{2N}$$

$$\tau_{Dout} = \lim_{N\to\infty} rcl^2 \frac{1+N}{2N} = \frac{rcl^2}{2} = \frac{RC}{2}$$

The delay of a wire is proportional to the square of its length.

Note: The Elmore formula applied to the RC lumped model gives $\tau_{Dout} = RC$

Source: Rabaey

RC delay – 5: The Elmore delay - 4

Example 4.8 of Rabaey's book: 10-cm-long, 1- μm-wide Al1 wire for which r=0.075 Ω/ μm, c= 110 aF/μm.

$$\tau_{Dout} = rcl^2/2 = 0.075\Omega/\mu\text{m} \cdot 110\text{aF}/\mu\text{m} \cdot \left(10^5\mu\text{m}\right)^2/2 = 41.3\text{ ns}$$

Note: The Elmore delay is, in general, not equal to the delay time. For a distributed RC network, the Elmore delay τ_D = 0.5 RC whereas the delay time t_d = 0.38 RC

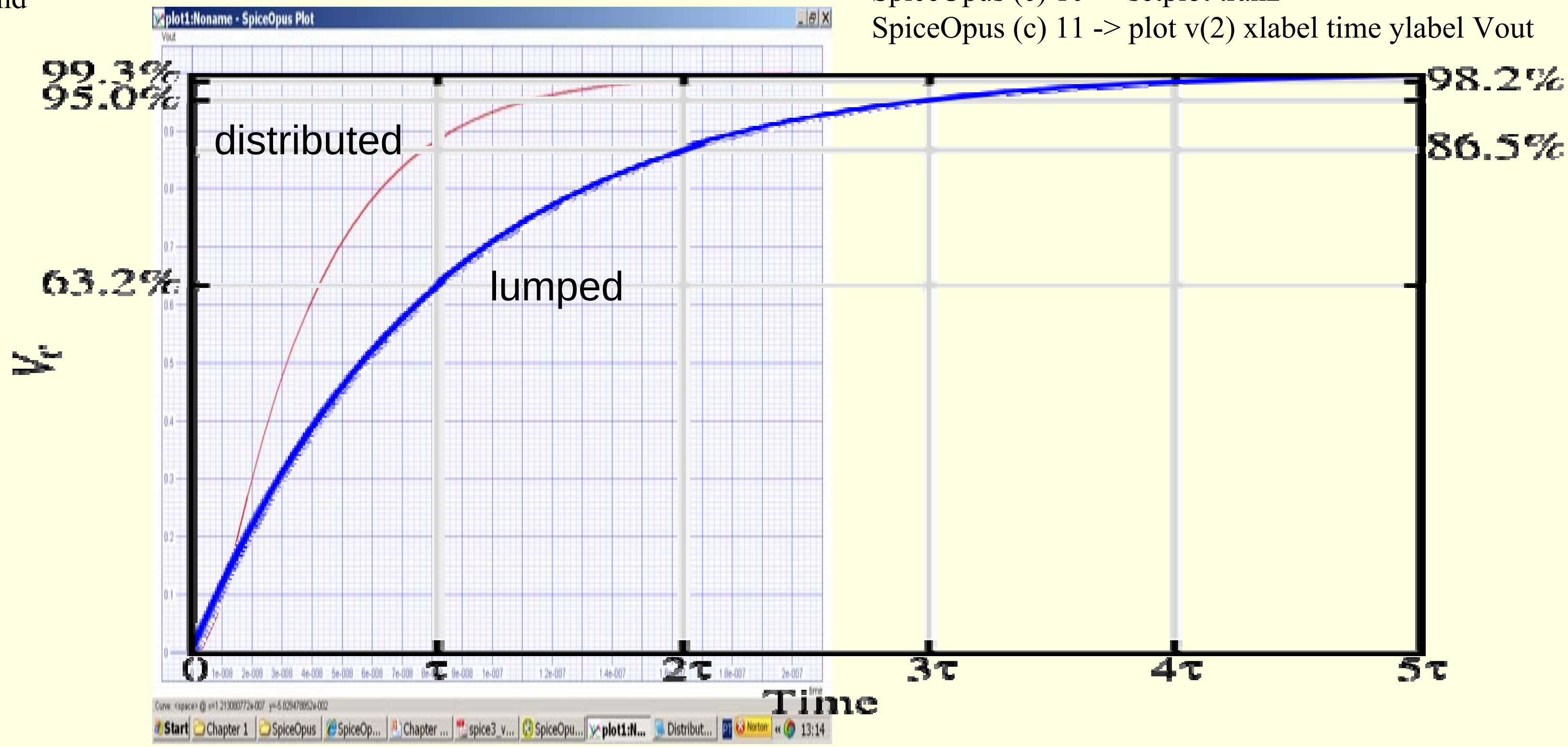
Source: Rabaey

RC delay – 6

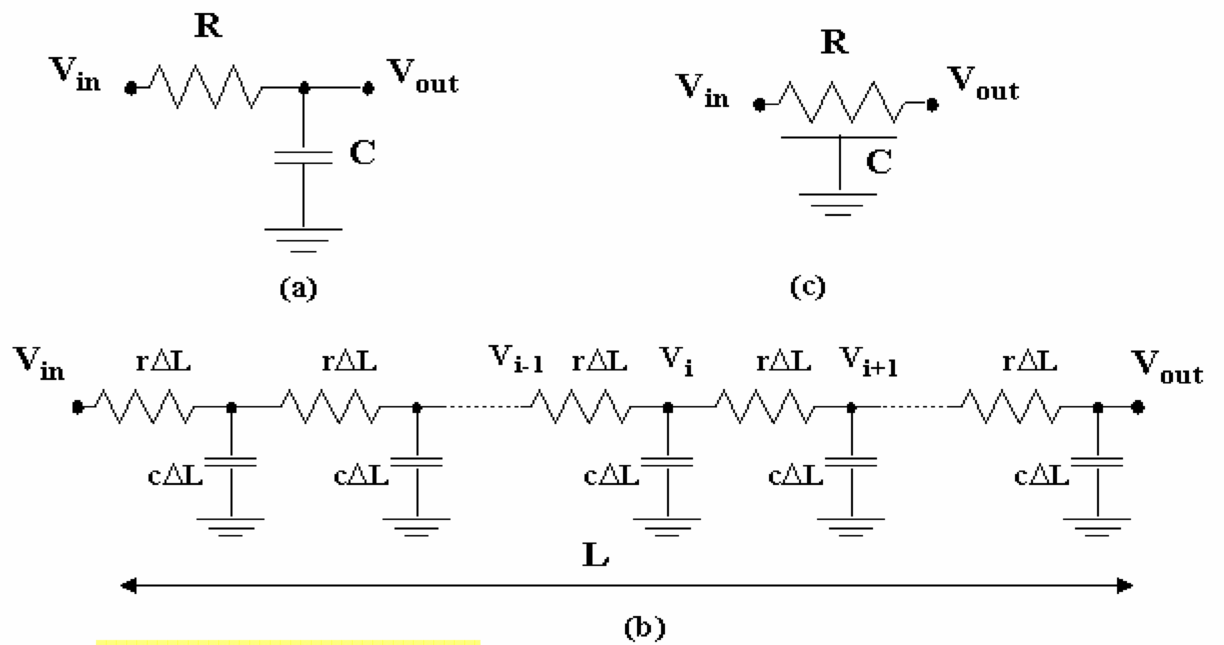
Example 4.8 of Rabaey's book: 10-cm-long, 1- μm-wide Al1 wire for which *r*=0.075 Ω/ μm, *c*= 110 aF/μm.

```
Distributed RC line 1
* this is DistributedRCline.cir file
v0 1 0 dc 0 pulse 0 1V 0 10ps 10ps 200ns 400ns
URC1 1 2 0 MURC L=100m
.model MURC URC rperl=75k cperl=110p
.end
```

```
SpiceOpus (c) 7 -> source DistributedRCline.cir
SpiceOpus (c) 8 -> tran 1ns 200ns
SpiceOpus (c) 9 -> setplot
                new              New plot
Current tran2   Distributed RC line 1 (Transient Analysis)
SpiceOpus (c) 10 -> setplot tran2
SpiceOpus (c) 11 -> plot v(2) xlabel time ylabel Vout
```



RC delay – 7



Diffusion equation

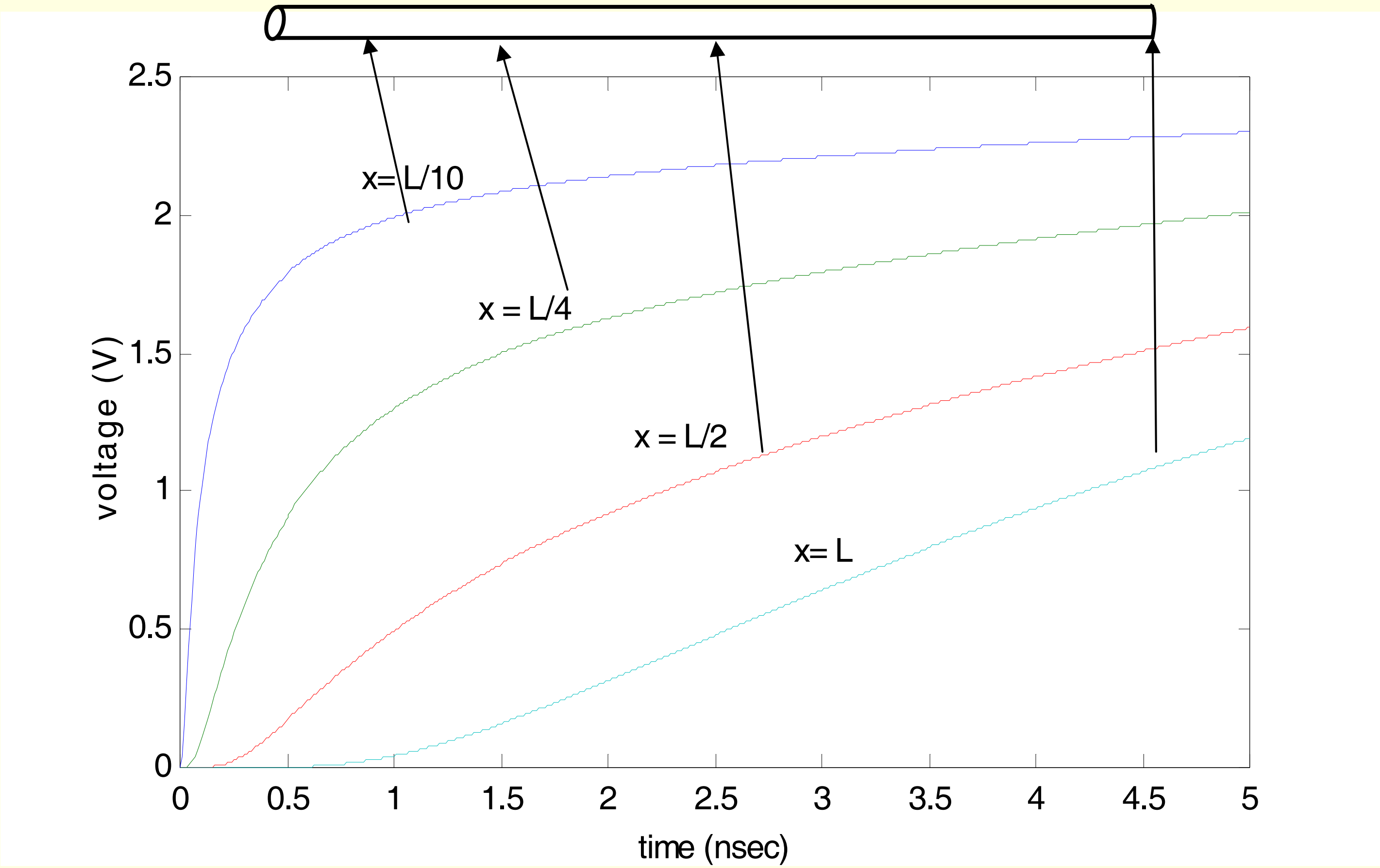
$$rc\frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2}$$

$$\tau(V_{out}) = \frac{rc\,L^2}{2}$$

Source: Rabaey

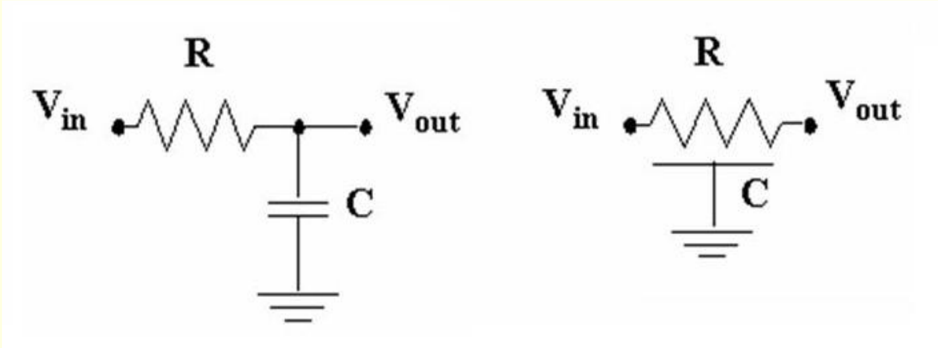
RC delay – 8

Step-response of RC wire as a function of time and space



Source: Rabaey

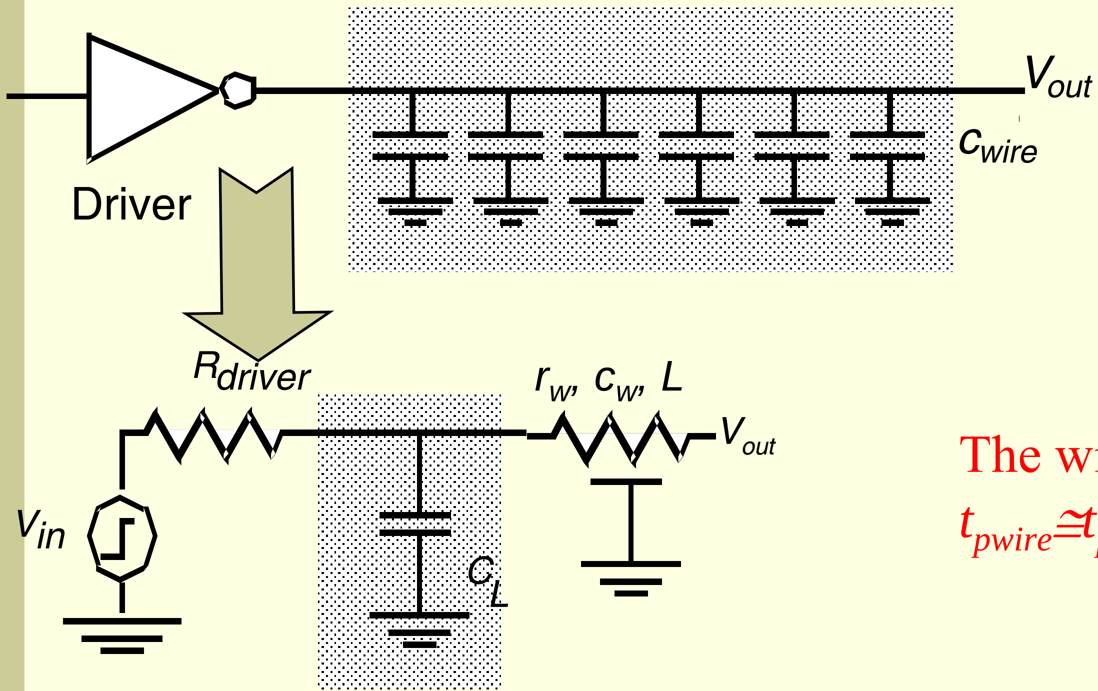
RC delay – 9



Voltage range	Lumped RC network	Distributed RC network
0→50% (t_p)	0.69 RC	0.38 RC
0→63% (τ)	RC	0.5 RC
10→90% (t_r)	2.2 RC	0.9 RC

Source: Rabaey

RC delay – 10



When are the effects of the wire delay important?

Assume that the driver delay is t_{pgate}. The wire delay is

$$t_{pwire} = 0.38RC = 0.38 r_w c_w L^2$$

The wire delay is important when $t_{pwire} \cong t_{pgate}$ or, equivalently

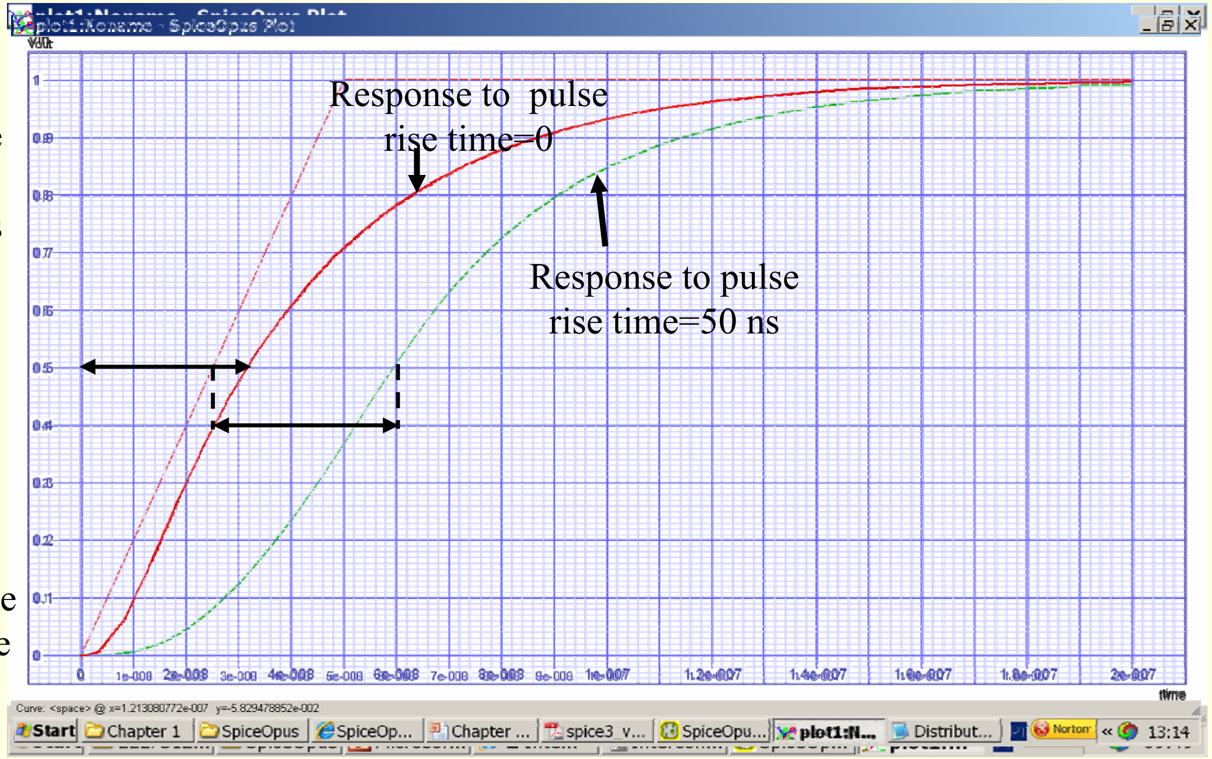
$$L_{crit} = \sqrt{\frac{t_{pgate}}{0.38 r_w c_w}}$$

Source: Rabaey

RC delay – 11

Example 4.8 of Rabaey's book: 10-cm-long, 1- µm-wide Al1 wire for which r=0.075 Ω/ µm, c= 110 aF/µm.

```
Distributed RC line 2
* this is DistributedRCline2.cir
*file
* the rise time is of the order of the
*RC time constant
v0 1 0 dc 0 pulse 0 1V 0 50ns 50ns
+200ns 500ns
URC1 1 2 0 MURC L=100m
.model MURC URC K=2
+fmax=20G rperl=75k cperl=110p
.end
```

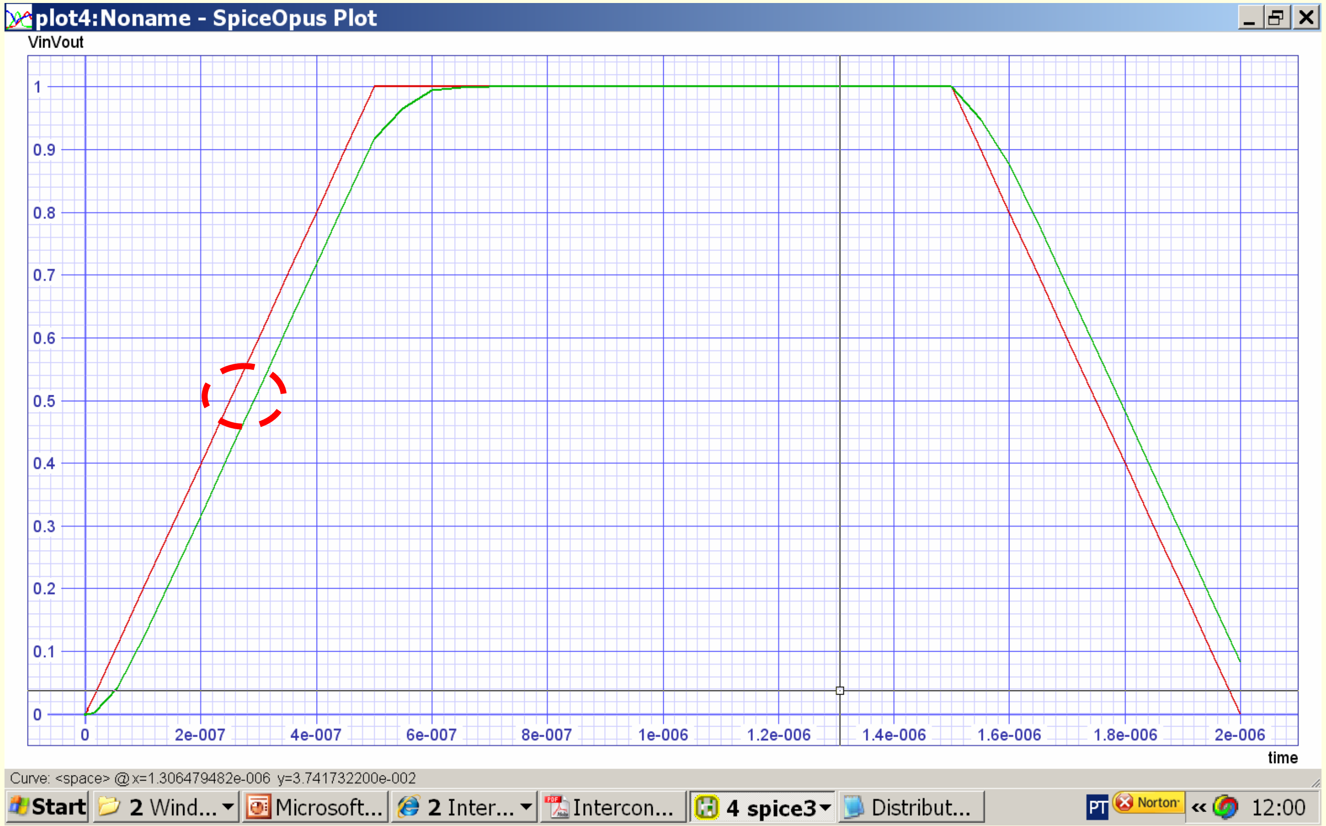


Note that the internal resistance of the voltage source is zero in this example

What if the rise time becomes much higher than RC?

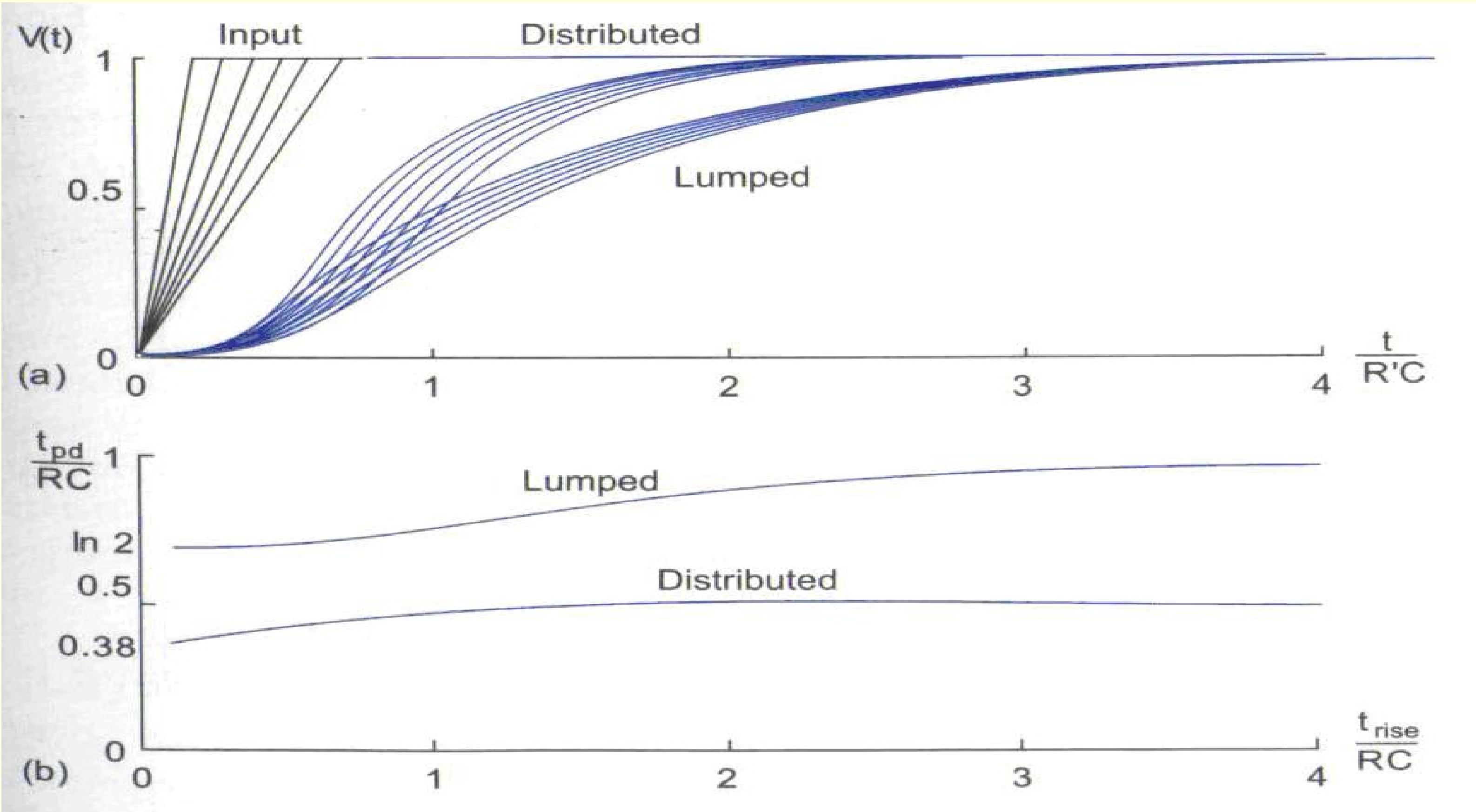
RC delay – 12

Example 4.8 of Rabaey's book: 10-cm-long, 1- µm-wide Al1 wire for which r=0.075 Ω/ µm, c= 110 aF/µm.



What if the rise time becomes much higher than RC?

RC delay – 13



Source: Weste&Harris

RC delay – 14

Design Rules of Thumb

- rc delays should only be considered when t_{pRC} >> t_{pgate} of the driving gate

$$L_{crit} \gg \sqrt{t_{pgate}/0.38rc}$$

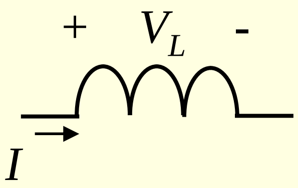
- rc delays should only be considered when the rise (fall) time at the line input is smaller than RC, the rise (fall) time of the line

$$t_{rise} < RC$$

  - when not met, the change in the signal is slower than the propagation delay of the wire

Source: Rabaey

Inductance - 1



$$V_L = L dI / dt$$

$$E_L = LI^2 / 2$$

Inductive effects

- ***important for power grids (high current), clock networks (high speed), and wide busses (low resistance/unit length);***
- ***may cause ringing/overshoot effects, reflection of signals, inductive coupling between lines (crosstalk), and switching noise in power lines***

Clock trees and power/ground grid need to be designed carefully to avoid large clock skew, signal inductive coupling and ground bounce

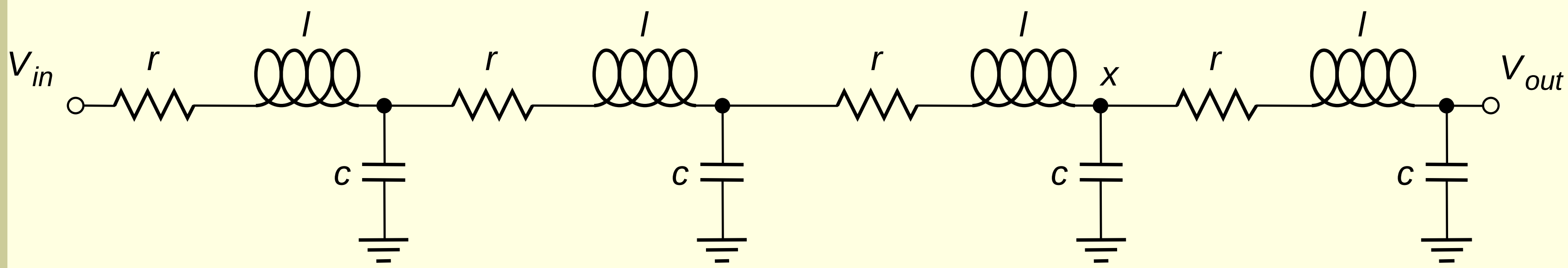
Inductance - 2

- ❖ **Inductance of a wire depends on its geometry and surrounding dielectric**
- ❖ **Extracting the inductance is in general a 3-D problem and is extremely time-consuming for complex geometries**
- ❖ **Inductance depends on the entire current loop; it is impractical to extract the inductance from a chip layout**

Source: Rabaey, Weste&Harris

Inductance - 3

The Transmission Line



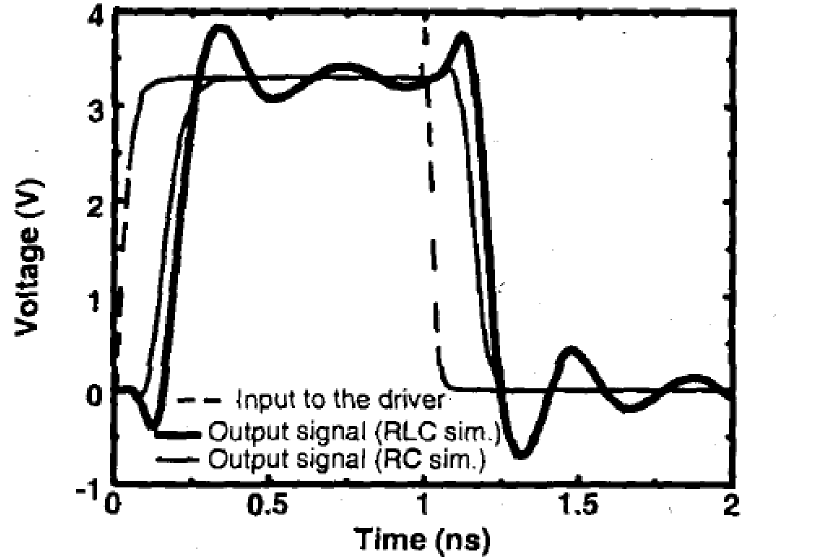
$$\frac{\partial^2 v}{\partial x^2} = rc\frac{\partial v}{\partial t} + lc\frac{\partial^2 v}{\partial t^2}$$

The Wave Equation

When r=0 → signal travels at speed of light, which is smaller than speed of light in vacuum (300 mm/ns). In the real case, currents return in distant power lines and increase inductance thus reducing signal velocity.
When l=0 → rc wire (diffusion equation)

Source: Rabaey

Inductance - 2



Signal wave forms at the output of receiver: ringing effects with RLC simulation.

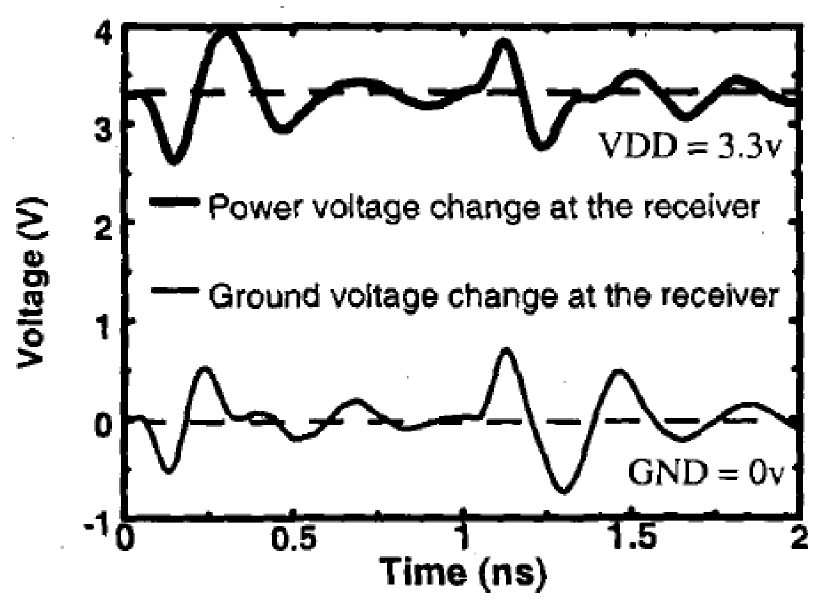


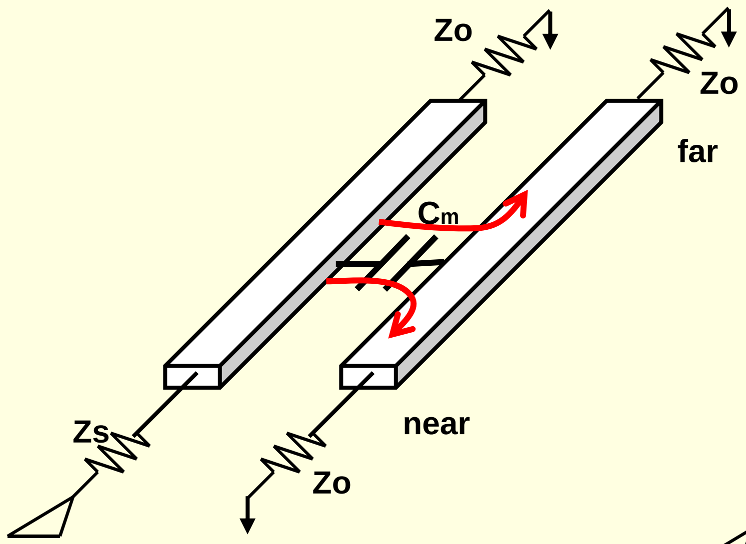
Fig. 10 Power and ground noise observed with RLC simulation.

Source: Qi, CICC 2000

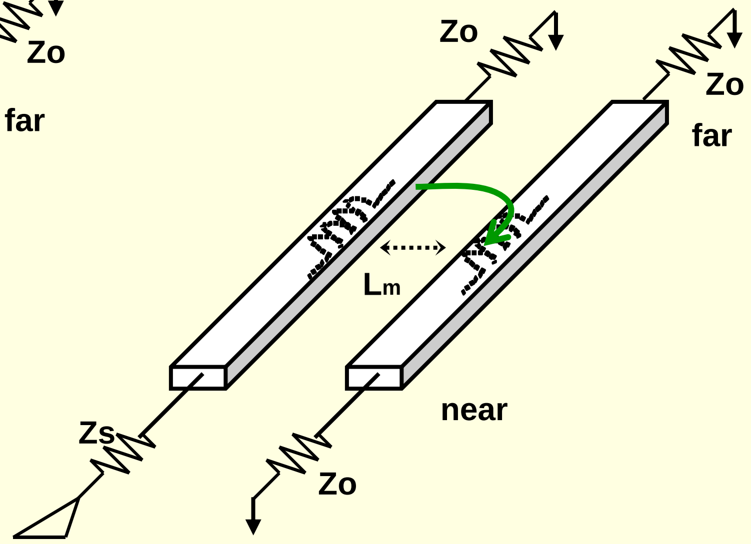
Crosstalk is the coupling of energy from one line to another via:

- ***Mutual capacitance (electric field)***
- ***Mutual inductance (magnetic field)***

Mutual Capacitance, C_m



Mutual Inductance, L_m



Source: Intel