Capacitance - 1

The parallel plate capacitor

Charge +Q
-Q
dielectric
Electric field E
Plate area A
Plate separation d
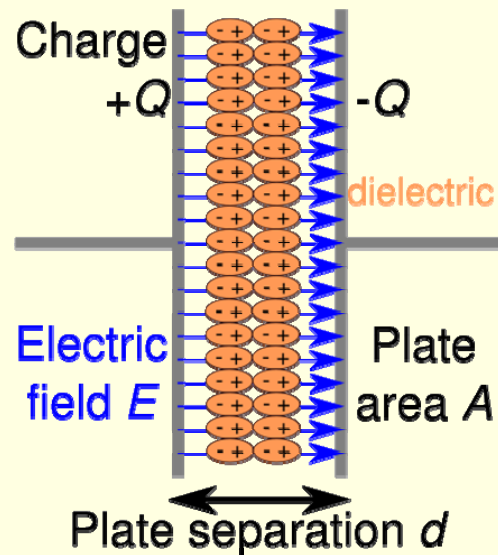
Capacitance: is a measure of the charge stored on each plate for a given voltage such that $Q=CV$

The electric field (force) E between the plates of a parallel plate capacitor is uniform and given by $E=V/d$
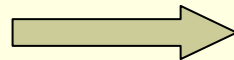
Charge separation in a parallel-plate capacitor causes an internal electric field. A polarized dielectric spacer (orange) reduces the electric field and increase the capacitance.

Source: wikipedia
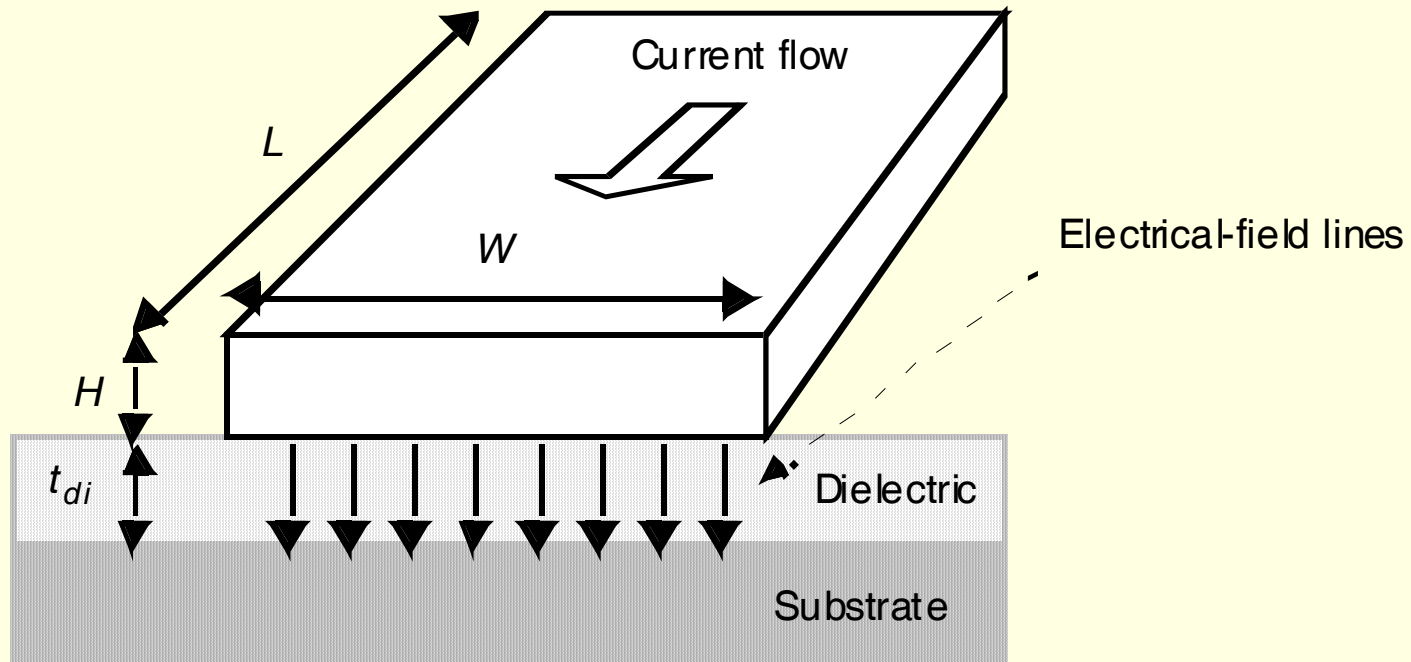
Capacitance - 2

$$c_{int} = \frac{\varepsilon_{di}}{t_{di}} WL$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \; \text{fF/}\mu\text{m}^2$$

Defined by foundry

Source: Rabaey

Capacitance - 3

Material	ε_r
Free space	1
Aerogels	~1.5
Polyimides (organic)	3-4
Silicon dioxide	3.9
Glass-epoxy (PC board)	5
Silicon Nitride (Si_3N_4)	7.5
Alumina (package)	9.5
Silicon	11.7

Source: Rabaey

Capacitance - 4

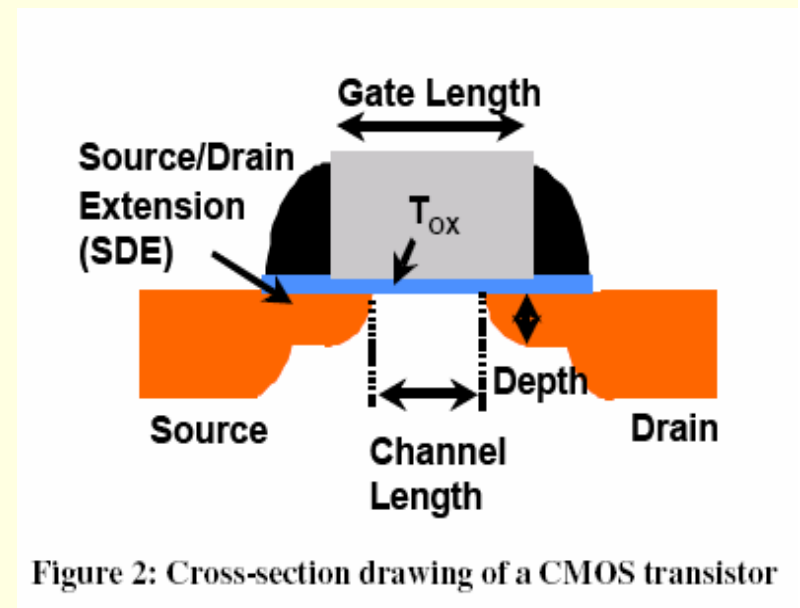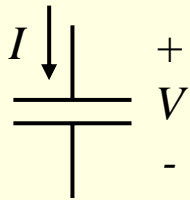| Fabrication process (CMOS)	Gate oxide thickness (nm)	Capacitance / area (fF/μm^2)
AMIS 1.5 μm	32	1.1
IBM 0.25 μm	6.3	5.5
IBM 0.13 μm	3.2	11

Figure 2: Cross-section drawing of a CMOS transistor

Source: MOSIS

Source: Intel Tech. Journal

Capacitance - 5

$$Q = CV; \qquad I = dQ/dt = d(CV)/dt$$

$$I = CdV/dt \qquad \text{for constant capacitance}$$

For constant $V \rightarrow I=0$, *i.e.* a capacitor behaves as an open circuit at dc.

Capacitors are energy-storage (memory) devices used in filters, oscillators, power sources.

Ideal capacitors are not dissipative (and not noisy) but charging and discharging them causes heating through dissipative devices connected to the capacitors.

The RC circuit - 1
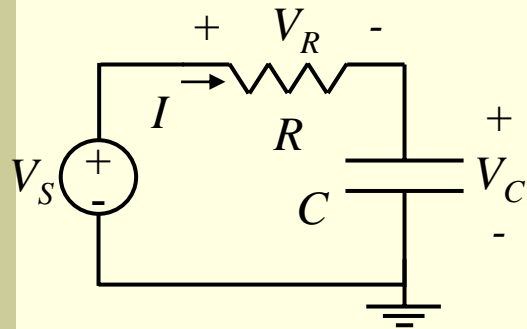
KCL $I = CdV_C/dt = V_R/R$

KVL $V_S = V_C + V_R$

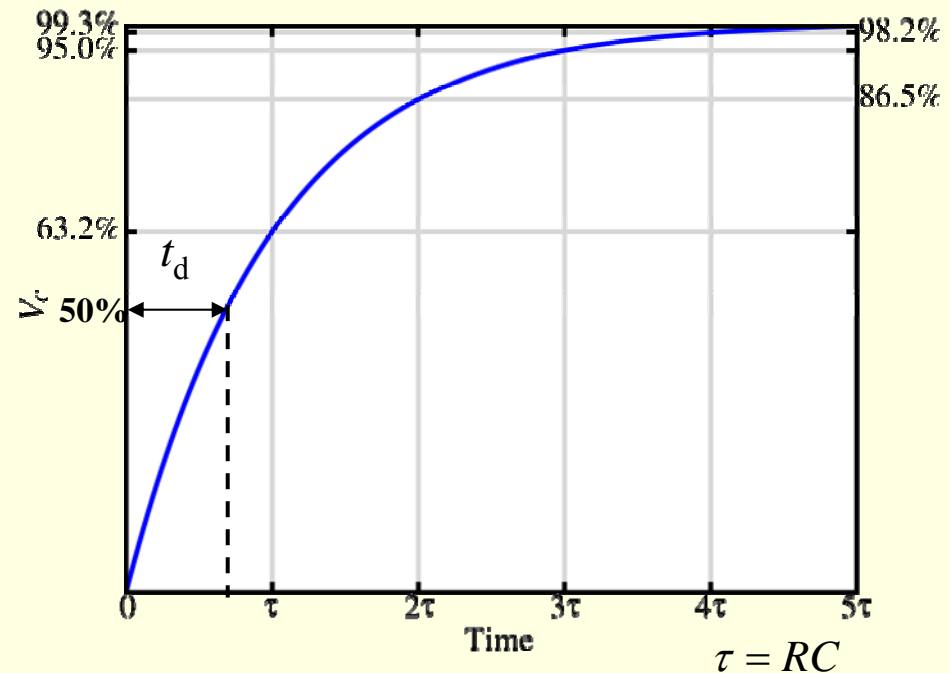$\left.\right\}V_S = RCdV_C/dt + V_C$

Assume that $V_S=0$ for $t<0$,
$V_S=A$ for $t\geq 0$ (and $V_C(0)=0$).

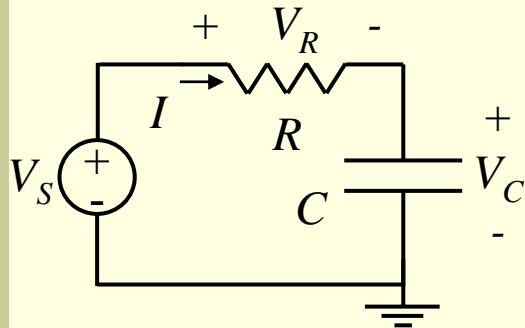$V_C = A\left[1 - \exp(-t/\tau)\right] \quad t \geq 0;$

$V_C = 0 \quad t < 0$

$I = CdV_C/dt = A\exp(-t/\tau)/R \quad t \geq 0$

$t_d = \tau\ln2 \cong 0.69\ \tau$

$\tau = RC$

The RC circuit - 2

Assume that $V_S=0$ for $t<0$,
$V_S=A$ for $t\geq0$ (and $V_C(0)=0$).

$$V_C = A\left[1-\exp(-t/\tau)\right] \qquad I = A\exp(-t/\tau)/R \quad t\geq 0$$

The power dissipation p (electric power converted into heat) in the resistor is

$$p = RI^2 = A^2\exp(-2t/\tau)/R$$

The energy converted into heat in the resistor is

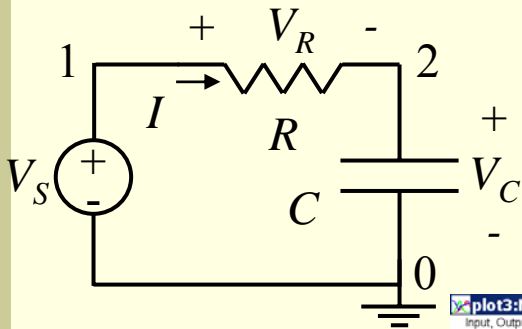$$E_R = \int_0^\infty p\,dt = \int_0^\infty \frac{A^2}{R}\exp\left(-\frac{2t}{\tau}\right)dt = \frac{CA^2}{2}$$

The energy stored in the capacitor (for t→∞)

$$E_C = \frac{CV_C^2}{2} = \frac{CA^2}{2}$$

Exercise: (a) Using the energy conservation principle calculate the energy delivered by the source. (b) Calculate the energy E_S delivered by the source using the formula below
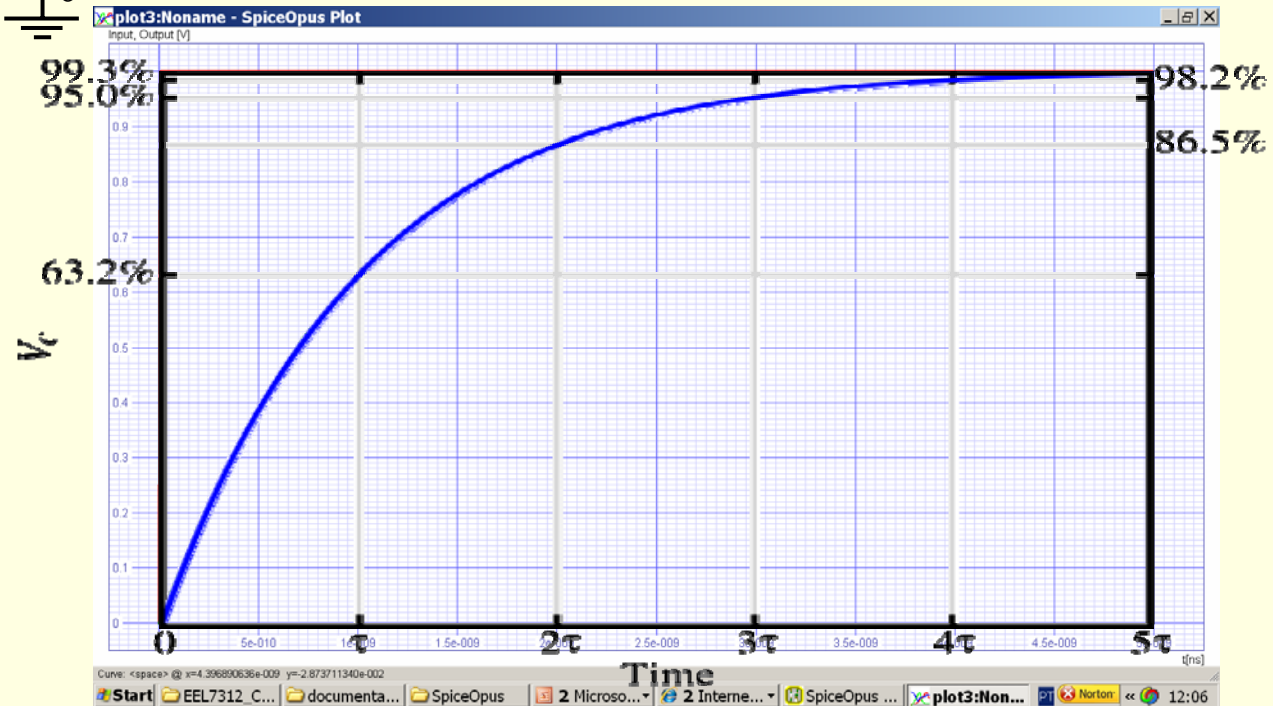
$$E_S = \int_0^\infty V_S I\,dt$$

Simulation 4.2

RC1
* this is RC1.cir file
v0 1 0 dc 0 pulse 0 1V 0 10ps 10ps 10ns 20ns
R 1 2 1k
C 2 0 1p
.end

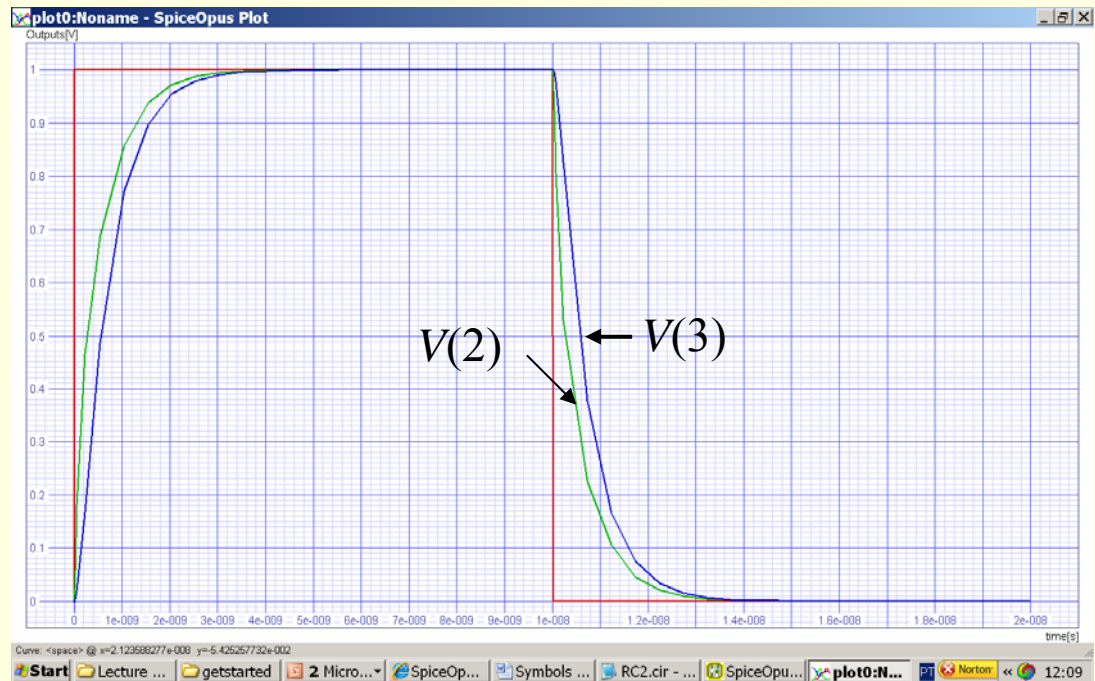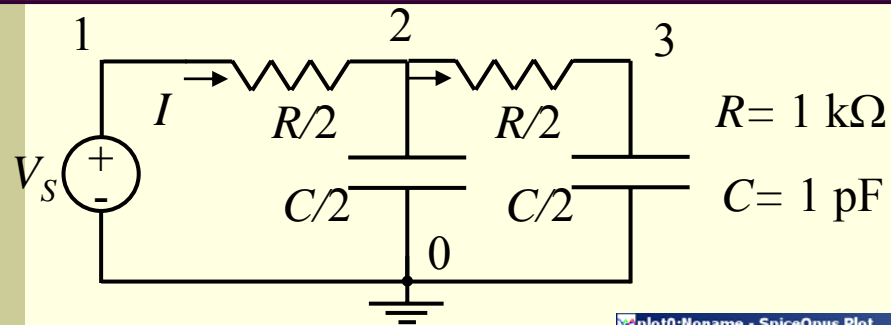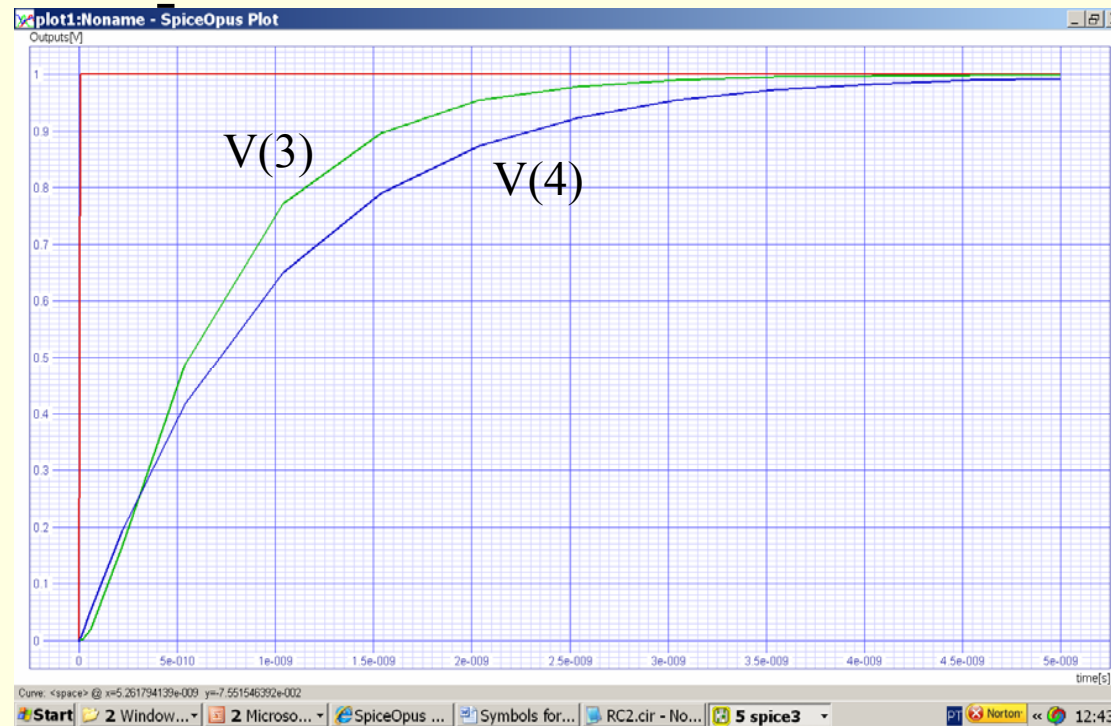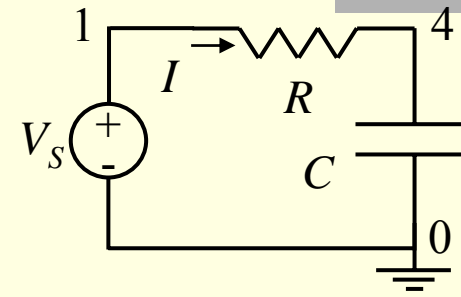**Exercise 4.2** Run SpiceOpus to determine the voltages at the intermediate nodes 2 and 3 for the stimulus of simulation 4.2

$R = 1\ k\Omega$

$C = 1\ pF$

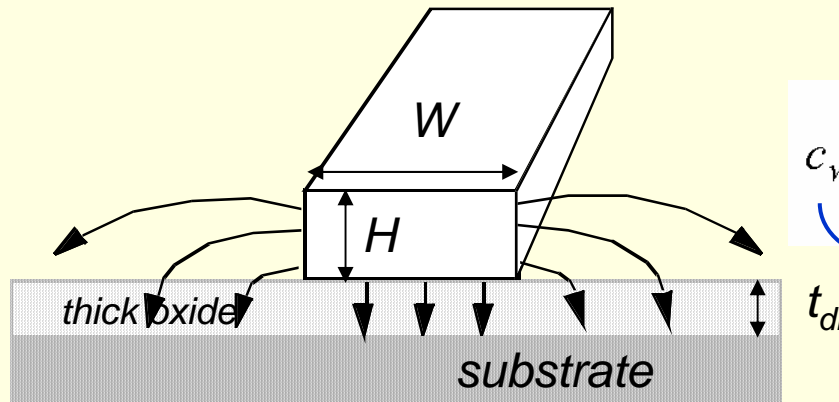# Comparison between exercises 4.1 and 4.2
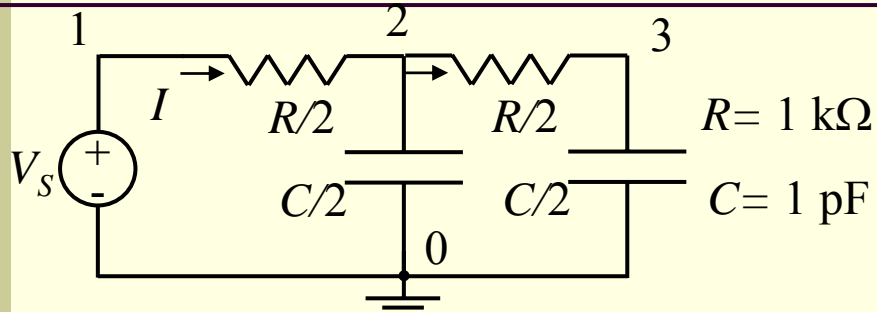
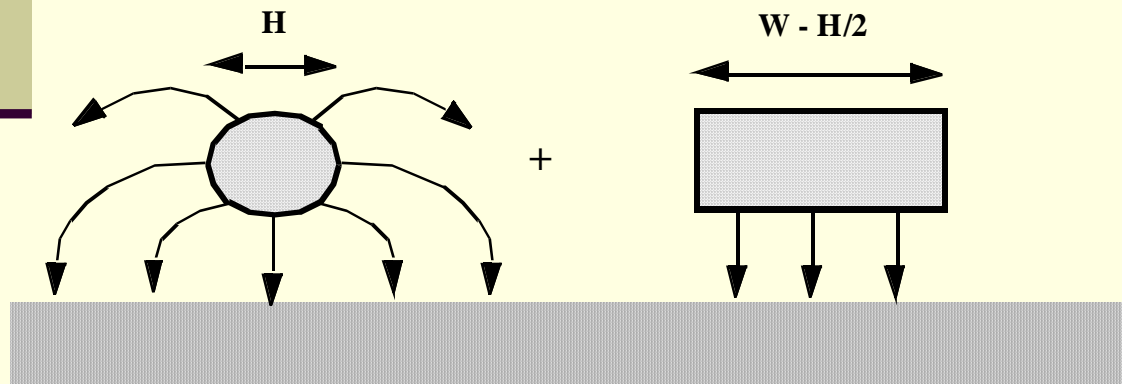# Capacitance - 6

Fringing Capacitance

$w = $ W-H/2

$$c_{wire} = c_{pp} + c_{fringe} = \frac{w\varepsilon_{di}}{t_{di}} + \frac{2\pi\varepsilon_{di}}{\log(t_{di}/H)}$$
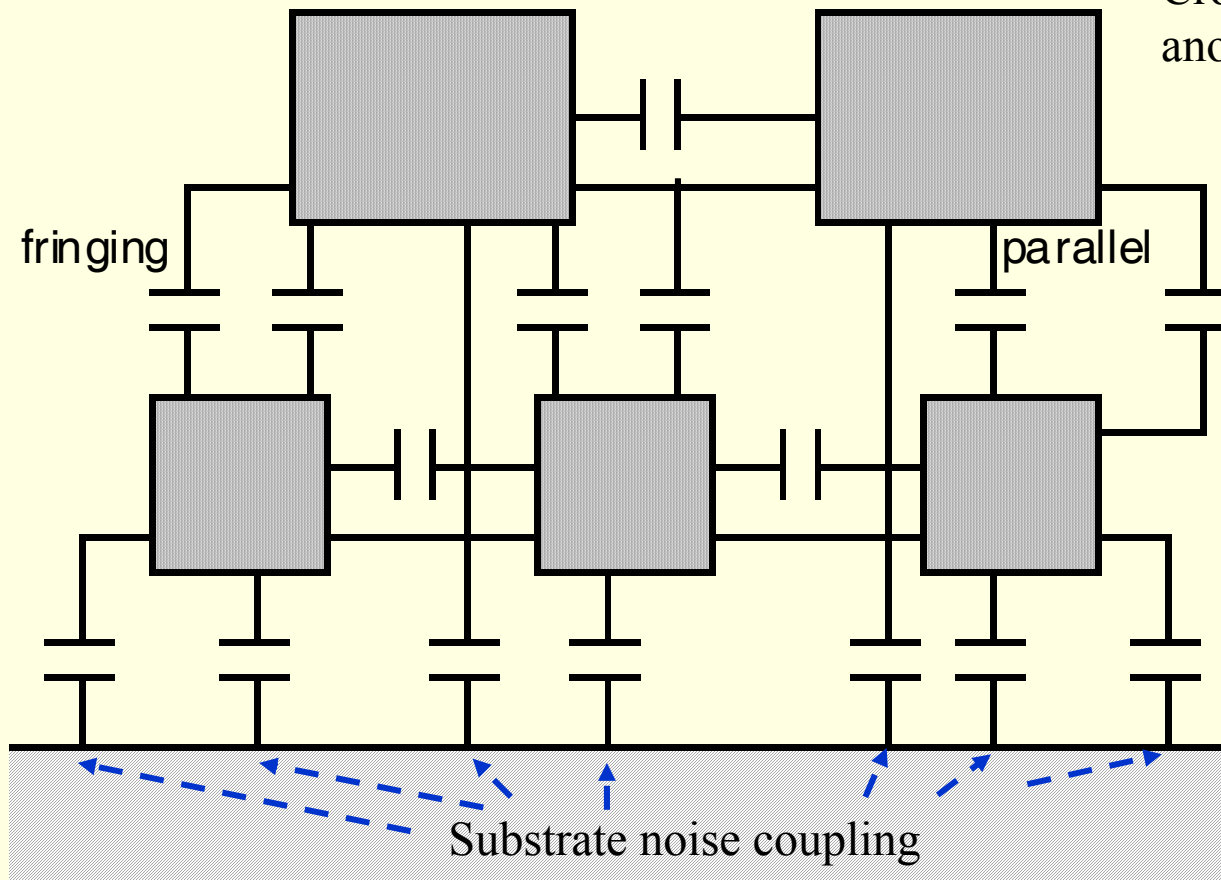
capacitance/unit length

(a)

(b)

Source: Rabaey

Capacitance - 7

Interwire Capacitance

Crosstalk: a signal can affect another nearby signal.

fringing

parallel

Substrate noise coupling

Capacitance - 8

Wiring Capacitances (0.25 μm CMOS)

|	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88						
	54						
Al1	30	41	57				
	40	47	54				
Al2	13	15	17	36			
	25	27	29	45			
Al3	8.9	9.4	10	15	41		
	18	19	20	27	49		
Al4	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	
Al5	5.2	5.4	5.4	6.6	9.1	14	38
	12	12	12	14	19	27	52

$aF/\mu m^2$

$aF/\mu m$

Source: Rabaey

Exercise 4.3

Estimate the capacitance of the wires specified below:
1. Polysilicon, W= 0.25µm, L=1 mm; 2. Polysilicon, W= 0.25µm, L=10 mm;
3. Metal 1, W= 0.25µm, L=1 mm;   4. Metal 1, W= 0.25µm, L=10 mm.

In each case, calculate the delay time assuming a lumped RC model for the wire and the capacitance with the substrate. Assume that the sheet resistances for polysilicon (with silicide) and metal 1 are 5 Ω and 0.1 Ω, respectively.

thick oxide
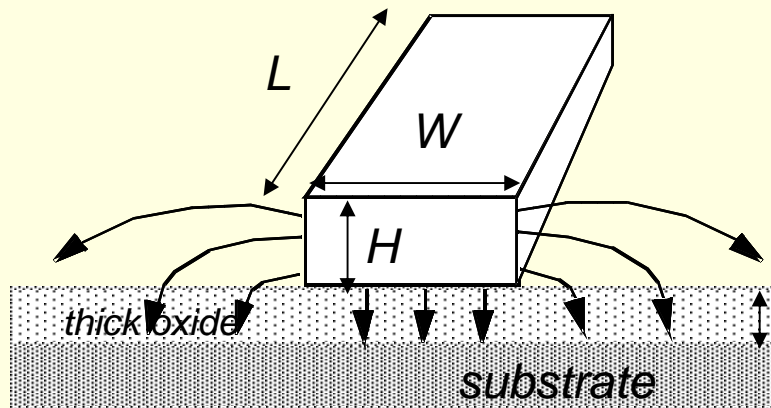
substrate

$$C_{PP} = \left(\frac{C_{PP}}{area} \right) WL; \quad C_{fringe} = \left(\frac{C_{fringe}}{length} \right) L$$

$$\frac{C_{PP}}{area} = 88 \text{ aF/µm}^2 \quad \frac{C_{fringe}}{length} = 54 \text{ aF/µm}$$

$$C_{wire} = C_{PP} + C_{fringe} \quad R_{wire} = R_\square \frac{L}{W}$$

$$t_d \cong 0.69 R_{wire} C_{wire}$$

$$c_{wire} = c_{pp} + c_{fringe}$$

Exercise 4.3 - Answer

1. C_{wire}=76 fF, R_{wire}= 20 kΩ, $R_{wire}C_{wire}$= 1520 ps, t_d=0.69$R_{wire}C_{wire}$=1050 ps

2. C_{wire}=760 fF, R_{wire}= 200 kΩ, $R_{wire}C_{wire}$= 152 ns, t_d=0.69$R_{wire}C_{wire}$=105 ns

3. C_{wire}=47.5 fF, R_{wire}= 400 Ω, $R_{wire}C_{wire}$= 19 ps, t_d=0.69$R_{wire}C_{wire}$=13 ps

4. C_{wire}=475 fF, R_{wire}= 4 kΩ, $R_{wire}C_{wire}$= 1.9 ns, t_d=0.69$R_{wire}C_{wire}$=1.3 ns

Note that the delay time increases proportionally with the square of the wire length. Why?
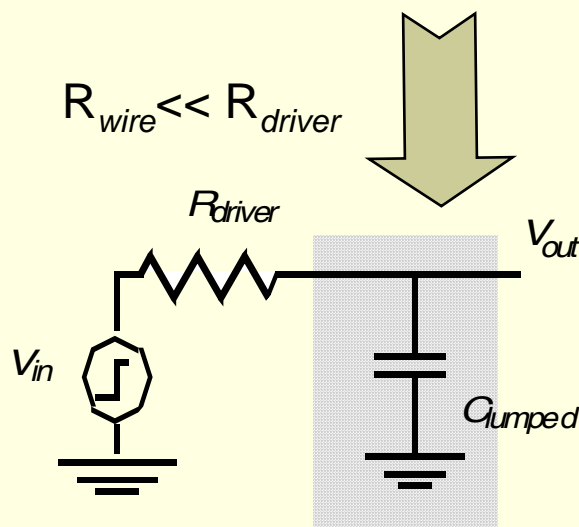
So far we have considered that the distributed RC line can be represented by a lumped RC model (pessimistic view) and that the drive signal is a step supplied by an ideal voltage source (optimistic view).

RC delay - 1

Influence of the output resistance of the driver
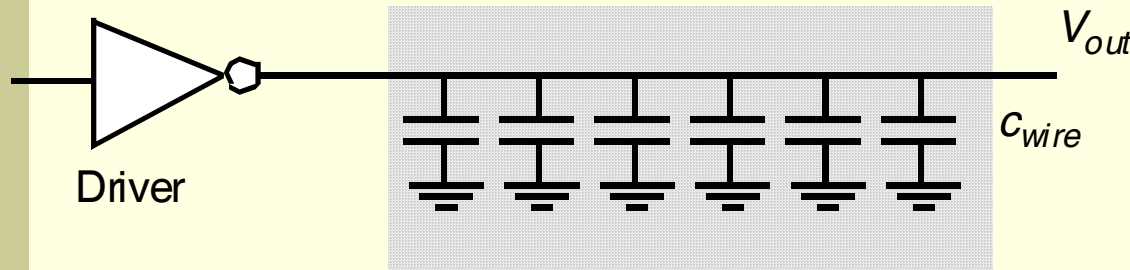
Example: R_{driver} =100 kΩ, and 1-μm-wide, 10-mm-long Al1 wire. What's t_{pd}?

$$\frac{C_{PP}}{area} = 30 \text{ aF/μm}^2 \qquad \frac{C_{fringe}}{length} = 40 \text{ aF/μm}$$

$$C_{PP} = \left(\frac{C_{PP}}{area}\right)WL = 0.3 \text{ pF}; \qquad C_{fringe} = \left(\frac{C_{fringe}}{length}\right)L = 0.4 \text{ pF}$$

$$C_{wire} = C_{PP} + C_{fringe} = 0.7 \text{ pF}$$

$$t_d \cong 0.69 R_{driver} C_{wire} \qquad\qquad t_d \cong 50 \text{ ns}$$

What's the approximate maximum operating frequency of the input such that the output can detect the correct value of the input?

Source: Rabaey

RC delay – 2: The Elmore delay -1

Elmore delay model *– method to determine the approximate delay time in an RC network; it avoids running costly simulations for calculation of delay time. Useful for determining delays in transmission lines, gates, clock distribution networks,…
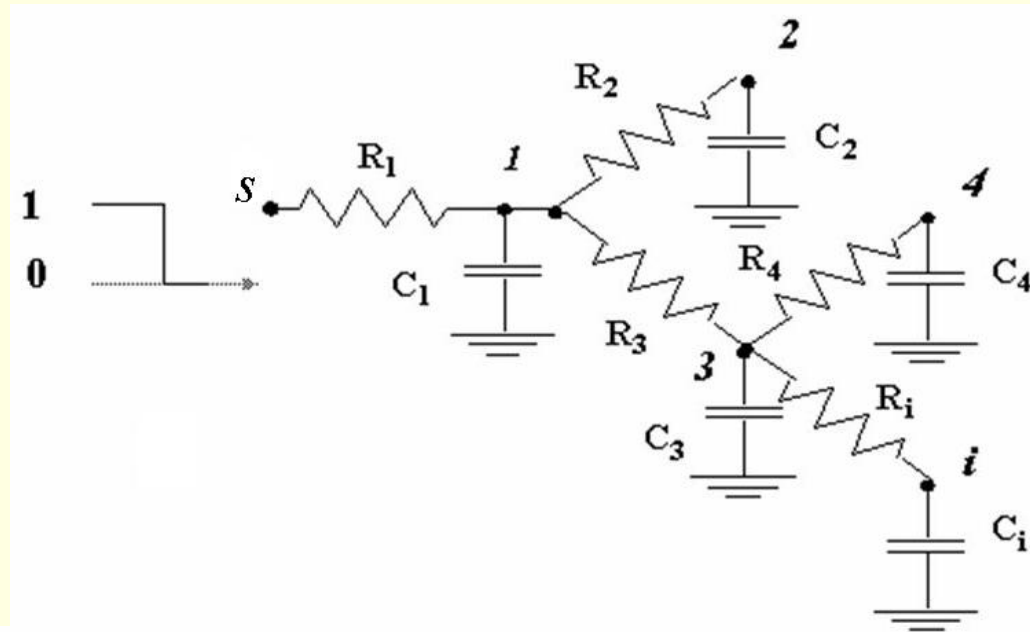
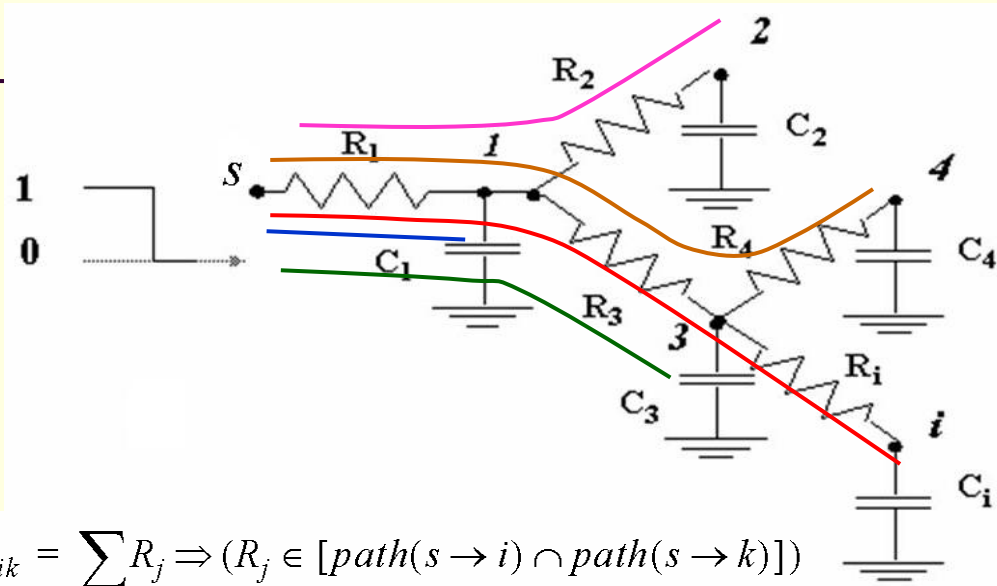
$$R_{ik} = \sum R_j \Rightarrow (R_j \in [path(s \rightarrow i) \cap path(s \rightarrow k)])$$

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik}$$

Sources: Rabaey & *W. C. Elmore, "The transient response of damped linear networks with particular regard to wideband amplifiers," J. Applied Physics, vol. 19, Jan 1948

RC delay – 3: The Elmore delay -2

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik}$$

$$R_{ik} = \sum R_j \Rightarrow (R_j \in [path(s \to i) \cap path(s \to k)])$$

$$\tau_{Di} = R_{i1}C_1 + R_{i2}C_2 + R_{i3}C_3 + R_{i4}C_4 + R_{ii}C_i =$$

—— path s→i $R_{ii}=R_1+R_3+R_i$ $(R_1 + R_3 + R_i)C_i +$

—— path s→1 $R_{i1}=R_1$ $R_1 C_1 +$

—— path s→2 $R_{i2}=R_1$ $R_1 C_2 +$

—— path s→3 $R_{i3}=R_1+R_3$ $(R_1 + R_3)C_3 +$

—— path s→4 $R_{i4}=R_1+R_3$ $(R_1 + R_3)C_4 +$