

Digital Integrated Circuits

Chapter 5 - Interconnections

Contents

- Introduction
- Resistance
- Capacitance
- RC delay
- Inductance
- Interconnection modeling
- Scaling effects on interconnection

Introduction - 1

Trend toward higher integration levels partially driven by faster, denser, and more reliable on-chip than off-chip interconnects.

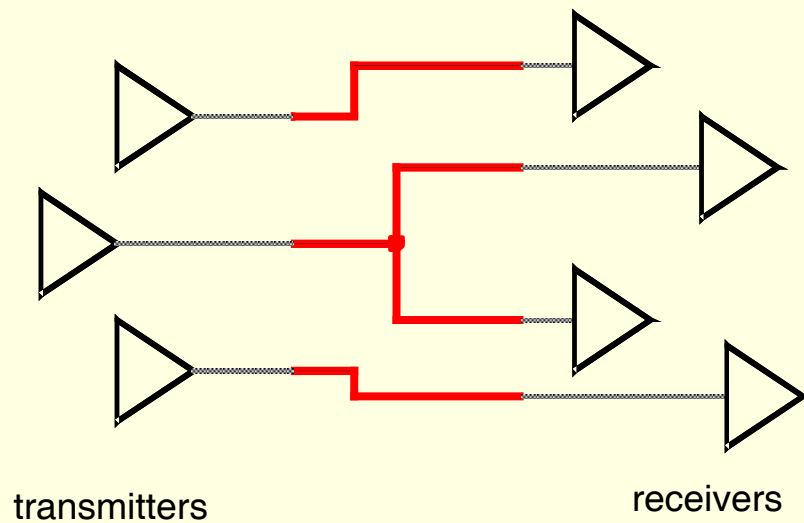
Why are on-chip interconnects important?

As technology scales to deep submicron:

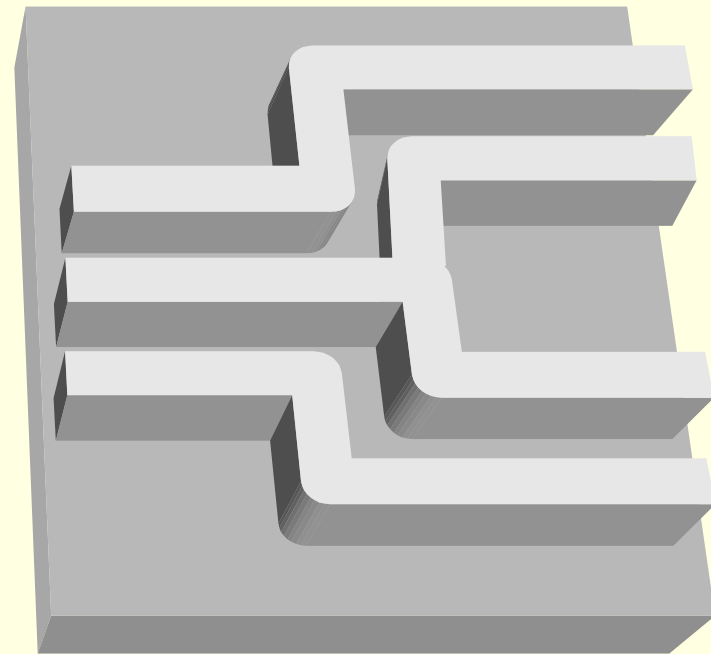
- Increased contribution to propagation delay
- Increased contribution on energy dissipation
- Introduces extra noise, affects reliability

Interconnect modeling: resistors, capacitors, and inductors.

Introduction - 2



schematics

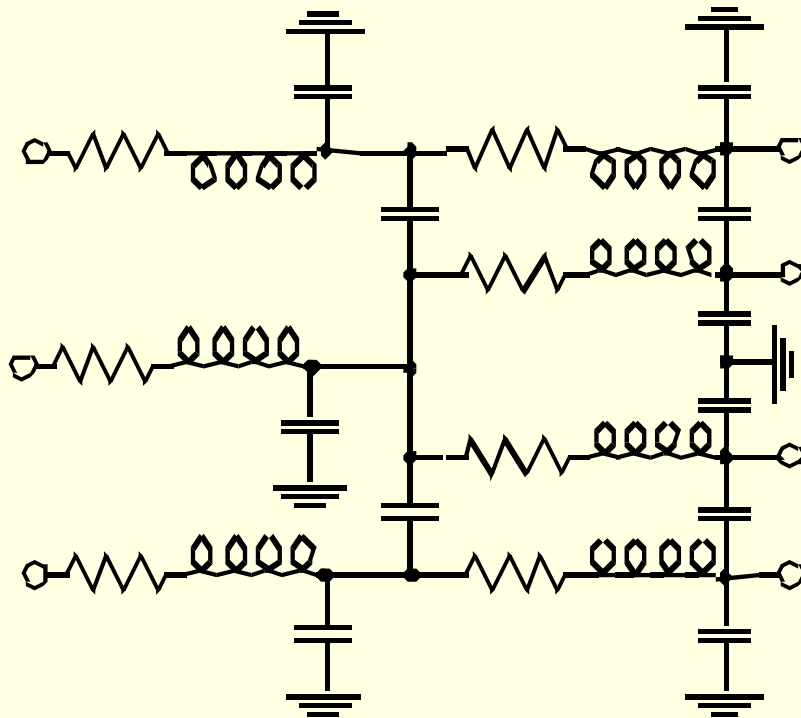


physical

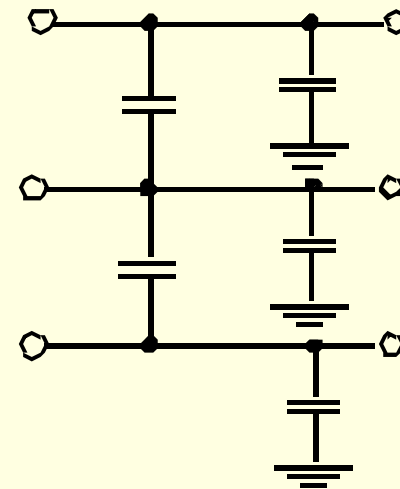
Source: Rabaey

Introduction - 3

Wire Models



All-inclusive model



Capacitance-only

Source: Rabaey

Introduction - 4

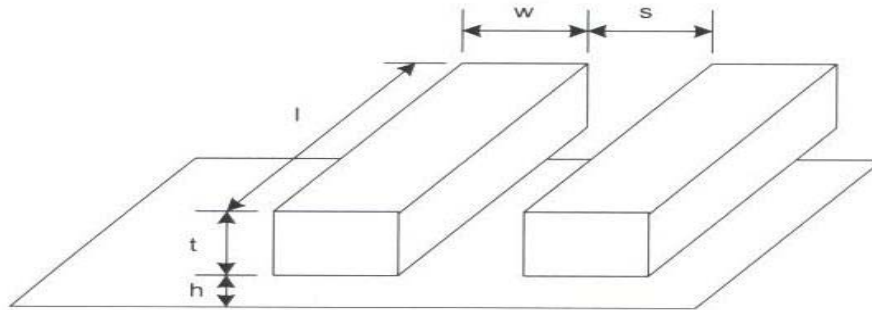
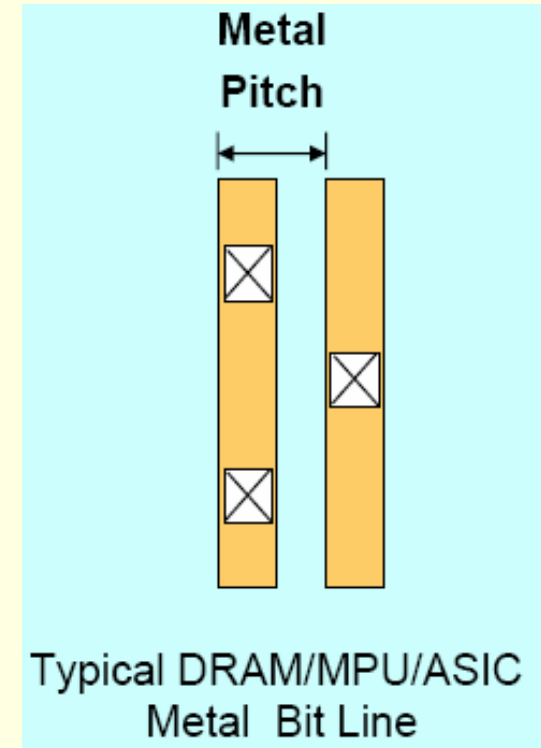


FIG 4.30 Interconnect geometry

Layer	t (nm)	w (nm)	s (nm)	AR	
6	1720	860	860	2.0	
	1000				
5	1600	800	800	2.0	
	1000				
4	1080	540	540	2.0	
	700				
3	700	320	320	2.2	
	700				
2	700	320	320	2.2	
	700				
1	480	250	250	1.9	
	800				

Substrate

FIG 4.31 Layer stack for 6-metal Intel 180 nm process



Introduction - 5

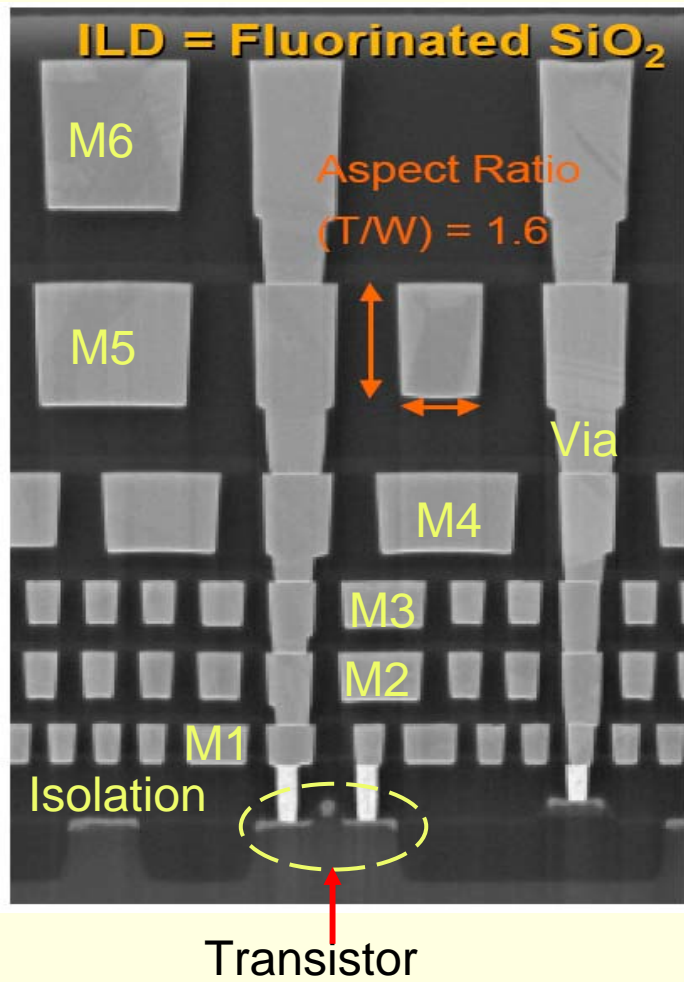
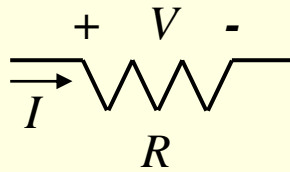


Table 1: Layer pitch, thickness (nm) and aspect ratio
130 nm CMOS technology (Intel)

<u>LAYER</u>	<u>PITCH</u>	<u>THICK</u>	<u>AR</u>
Isolation	345	450	-
Polysilicon	319	160	-
Metal 1	293	280	1.7
Metal 2,3	425	360	1.7
Metal 4	718	570	1.6
Metal 5	1064	900	1.7
Metal 6	1143	1200	2.1

Resistance - 1

Ohm's law



$$I = V / R$$

Defined by manufacturer

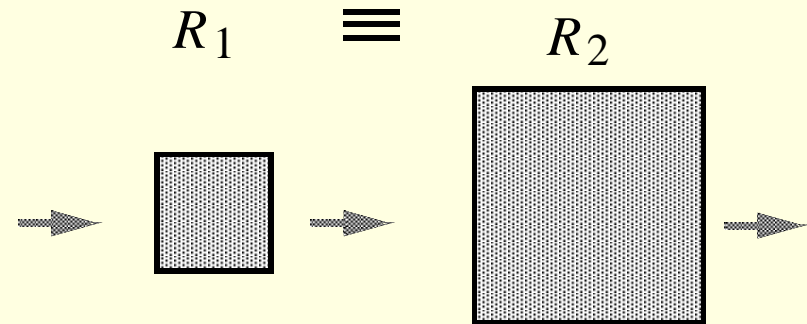
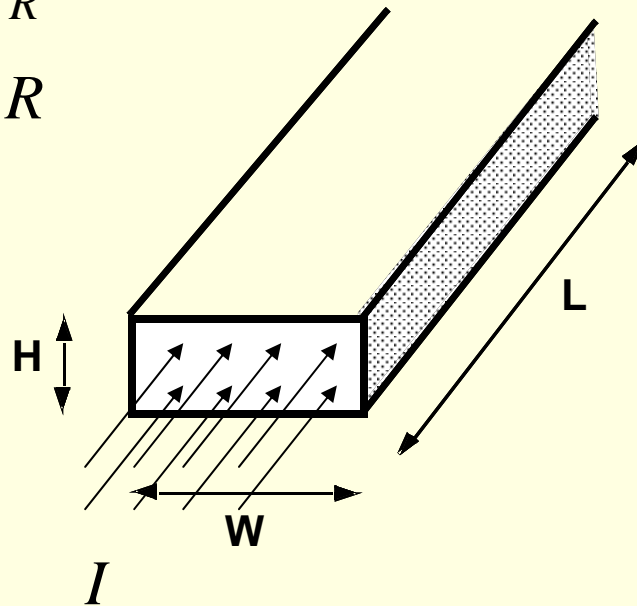
Material property

Height

$$R = \frac{\rho L}{HW} = R_{\square} \frac{L}{W}$$

Defined by designer (sometimes)

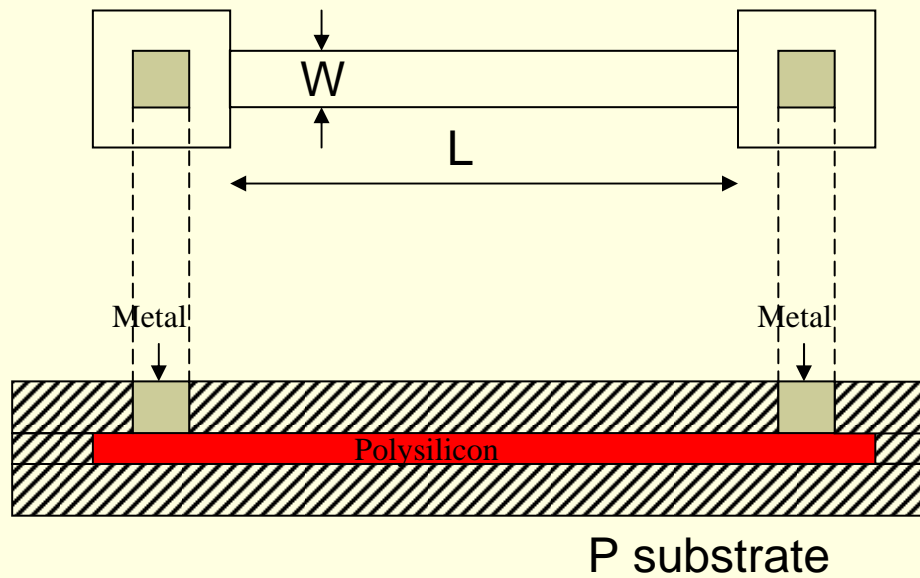
R_{\square} : sheet resistance



Resistance - 2

Material	ρ ($\Omega\text{-m}$)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

Resistance - 3



Ex: Poly-resistor

$$R = R_{\square} \frac{L}{W} + 2R_H$$

R_{\square} : sheet resistance

R_H : head resistance

Resistance - 4

Material	Sheet Resistance (Ω/\square)
n- or p-well diffusion	1000 – 1500
n^+ , p^+ diffusion	50 – 150
n^+ , p^+ diffusion with silicide	3 – 5
n^+ , p^+ polysilicon	150 – 200
n^+ , p^+ polysilicon with silicide	4 – 5
Aluminum	0.05 – 0.1

Sheet resistance values for a typical 0.25 μm CMOS process

Example: Calculate the approximate resistance of a 1 μm -wide, 1 mm-long wire of (a) polysilicon; (b) aluminum. Use the data of the above table.

Circuit Simulation - 1

Why using circuit simulators?

Designs can be quickly evaluated without (sometimes very expensive) fabrication.

After design has been evaluated you can prototype it before mass production.

A circuit simulator computes the response of the circuit to a particular stimulus. The simulator formulates the circuit equations and then numerically solves them.

Types of analyses:

- **DC/DC sweep: Both stimuli and responses do not vary with time**
- **Transient: Responses vary with time**
- **AC/Noise: also called small-signal analysis, it computes the sinusoidal steady-state response**

Circuit Simulation - 2

What are the input data?

Device Type (R, C, L, current sources, voltage sources, diodes, transistors)

Device models/parameters/ dimensions

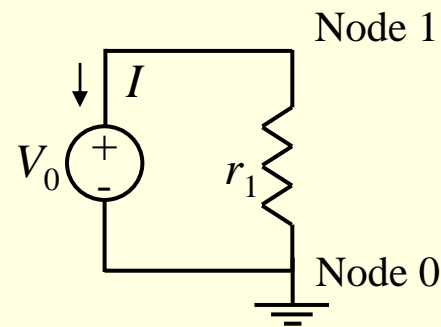
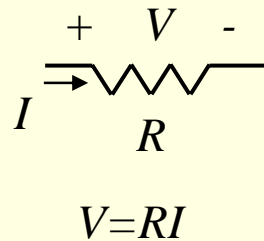
How devices are connected

Some circuit simulators:

SPICE, PSPICE, HSPICE, Spectre, Smash, SPiceOpus,....

Simulation 4.1

Use SpiceOpus to determine the (dc) I-V characteristic of a 1 kΩ resistor.



```
resistortest
* this is resistortest.cir file
v0 1 0 dc 10V
r1 1 0 1k
.end
```

SpiceOpus (c) 1 -> source resistortest.cir

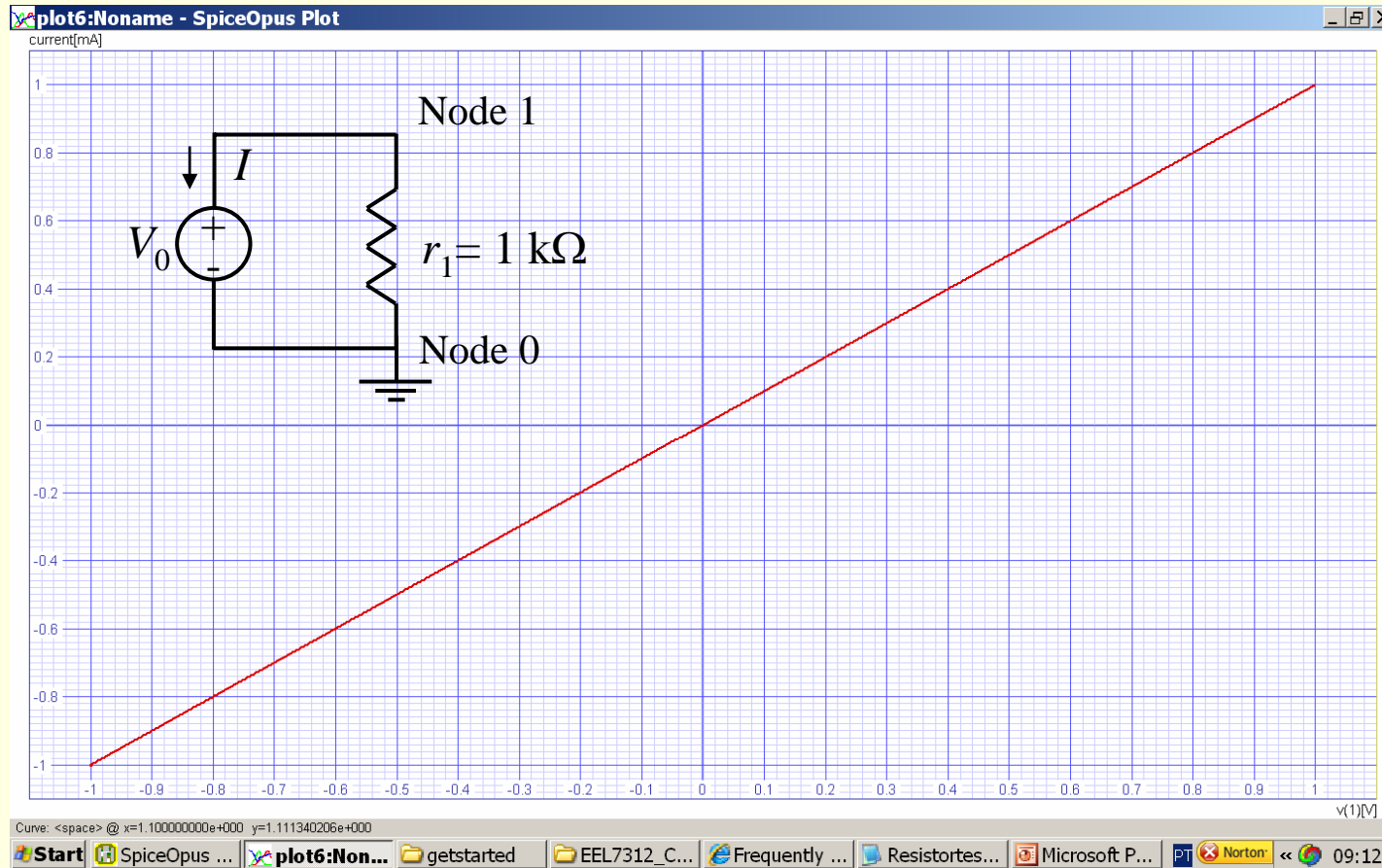
SpiceOpus (c) 2 -> dc v0 -1V 1V 2mV

SpiceOpus (c) 3 -> setplot dc1

SpiceOpus (c) 4 -> plot i(v0) xlabel v(1) ylabel current[A]

SpiceOpus (c) 5 -> plot -1000*i(v0) xlabel v(1) ylabel current[mA]

Simulation 4.1



Exercise 4.1 Use SpiceOpus to determine the (dc) I - V_0 transfer characteristic of the circuit given below.

