



Universidade Federal de Santa Catarina
Centro Tecnológico
Departamento de Informática e Estatística
Curso de Graduação em Ciências da Computação



Sistemas Digitais

INE 5406

Aula 2-P

Simulação *gate-level* de um somador completo com o ModelSim.

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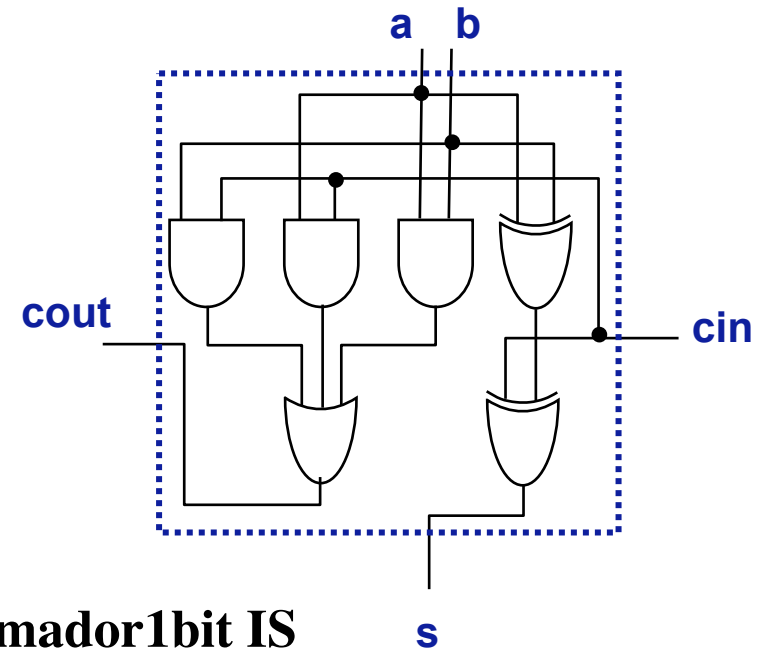
www.inf.ufsc.br/~guntzel/ine5406/ine5406.html

Introdução à Linguagem VHDL

▶ Exemplo: um Full Adder

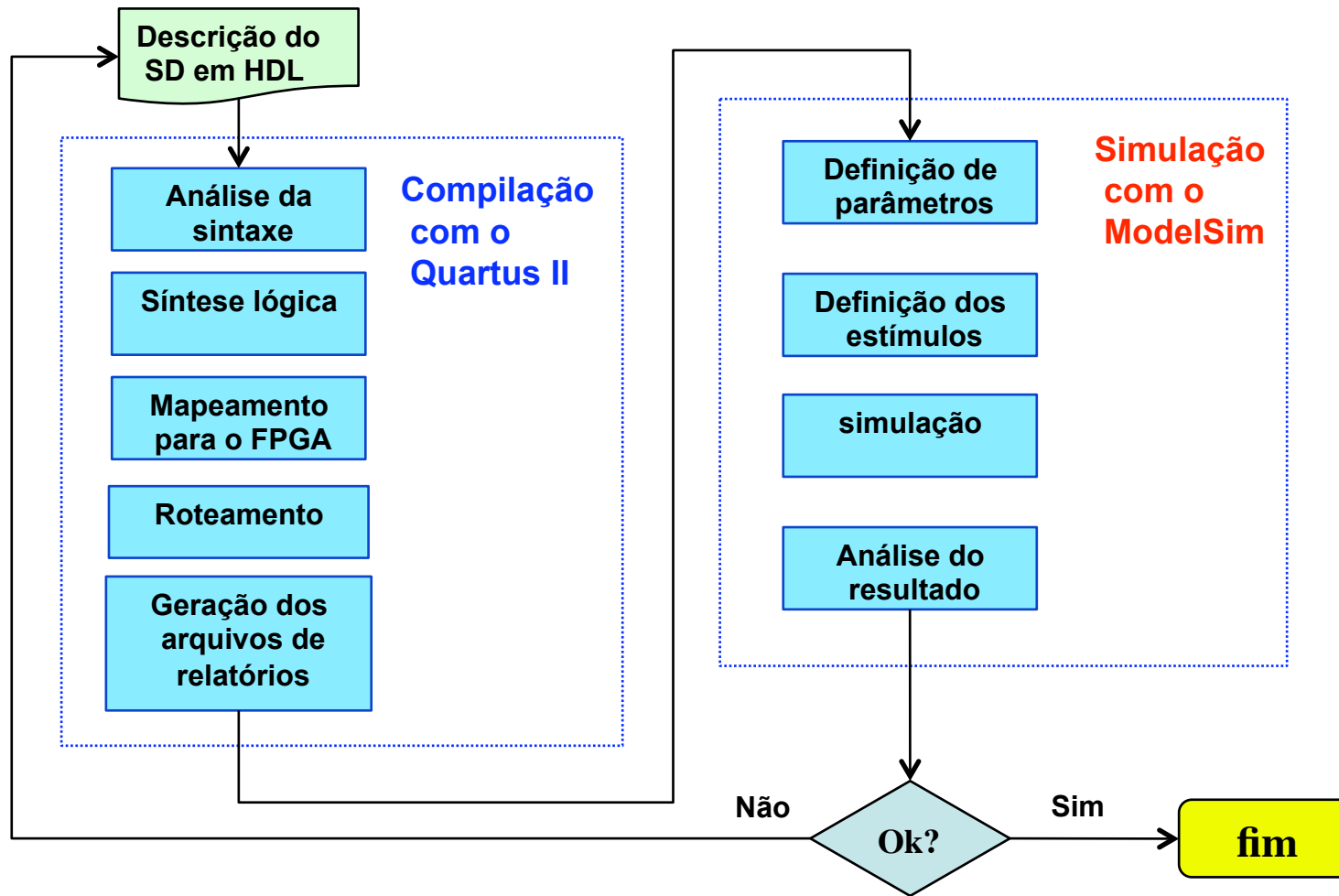
```
LIBRARY ieee;  
USE ieee.std_logic_1164.all;  
  
ENTITY somador1bit IS  
    PORT (cin, a, b : IN STD_LOGIC;  
          s, cout : OUT STD_LOGIC);  
END somador1bit ;
```

```
ARCHITECTURE comportamento OF somador1bit IS  
BEGIN  
    s <= a XOR b XOR cin;  
    cout <= (a AND b) OR (a AND cin) OR (b AND cin);  
END comportamento;
```



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► Fluxo de Projeto para FPGAs



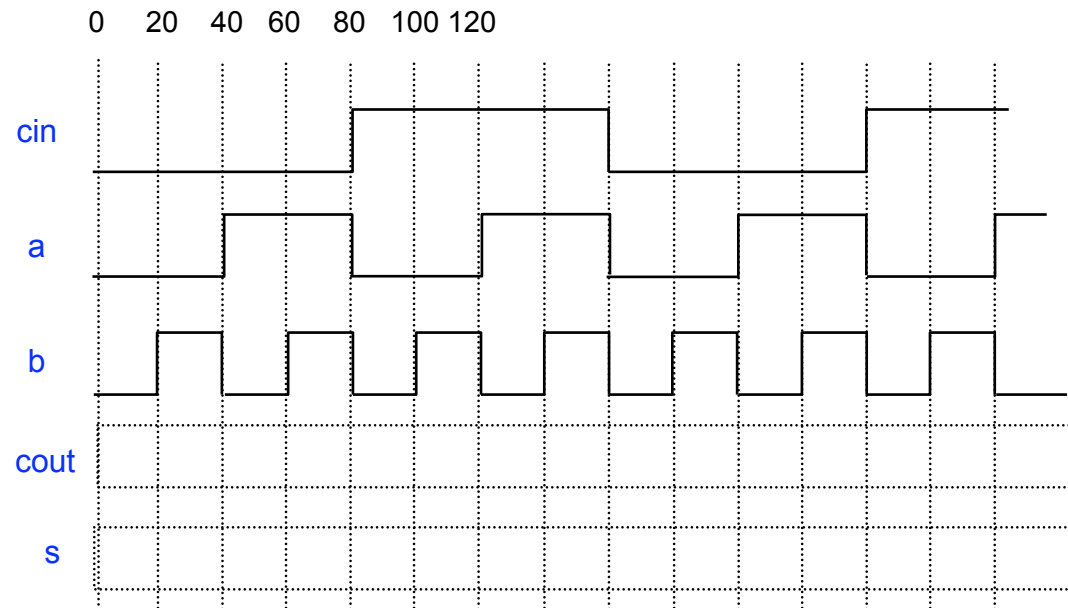
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▶ **Experimento 1:** descrição/compilação e simulação de um SC

Preparação dos Estímulos para a Simulação

Solução trivial (ingênua): Transformar a tabela-verdade em formas de onda

cin	a	b	cout	s
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



Observações:

1. Preencher a mão as waveforms (formas de onda) esperadas para as saídas para confrontá-la com o resultado da simulação.
2. T deve ser maior que “longest tpd” reportado pelo Quartus II.

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▶ **Experimento 1:** descrição/compilação e simulação de um SC

- A verificação será feita por meio de simulação no nível lógico com atrasos com a ferramenta ModelSim da Mentor Graphics, versão Altera. (O ModelSim chama este tipo de simulação de “*gate level simulation*”.)
- As próximas transparências mostram como configurar o ModelSim-Altera e como realizar a simulação.

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► Definir o caminho do Modelsim-Altera

The image shows the Quartus II software interface with the 'Options' dialog box open. The 'EDA Tool Options' section is selected, and the 'ModelSim-Altera' entry in the table is highlighted. A yellow callout box points to the path 'C:\altera\91\modelsim_ase\win32aloem'.

EDA Tool	Path
ModelSim	< double-click to change path >
ModelSim-Altera	C:\altera\91\modelsim_ase\win32aloem
NCSim	< double-click to change path >

Diretório Padrão:
"C:\altera\91\modelsim_ase\win32aloem"

Obs: é possível que o caminho para o ModelSim-Altera já esteja definido.

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▶ Abrir a ferramenta Modelsim-Altera

The screenshot displays the Quartus II software interface. The main window title is "Quartus II - H:/Sistemas_Digitais/Somador1Bit/somador1bit - somador1bit - [Compilation Report - Timing Analyzer Summary]". The menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. The Tools menu is open, showing options like "Run EDA Simulation Tool", "Run EDA Timing Analysis Tool", "Launch EDA Simulation Library Compiler", "Launch Design Space Explorer", "TimeQuest Timing Analyzer", "Advisors", "Chip Planner (Floorplan and Chip Editor)", "Design Partition Planner", "Netlist Viewers", "SignalTap II Logic Analyzer", "In-System Memory Content Editor", "Logic Analyzer Interface Editor", "In-System Sources and Probes Editor", "SignalProbe Pins...", "Programmer", "MegaWizard Plug-In Manager...", "SOPC Builder", "Tcl Scripts...", "Customize...", "Options...", "License Setup...", "Customize Compilation Report...", and "Options for Report Window...". The "Run EDA Simulation Tool" option is selected, and its sub-menu is open, showing "EDA RTL Simulation" and "EDA Gate Level Simulation...".

The Project Navigator on the left shows a file named "somador1bit.vhd". The Tasks window shows a list of tasks with their completion status and time taken:

Task	Time
Compile Design	00:00:25
Analysis & Synthesis	00:00:04
Fitter (Place & Route)	00:00:11
Assembler (Generate programming files)	00:00:05
Classic Timing Analysis	00:00:02
EDA Netlist Writer	00:00:03
Program Device (Open Programmer)	

The message window at the bottom shows the following text:

```
Info: Command: quartus_tan --re
Info: Longest tpd from source p
Info: Quartus II Classic Timing
Info: *****
Info: Running Quartus II EDA Netlist Writer
```

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▶ Iniciar simulação “Gate-Level”

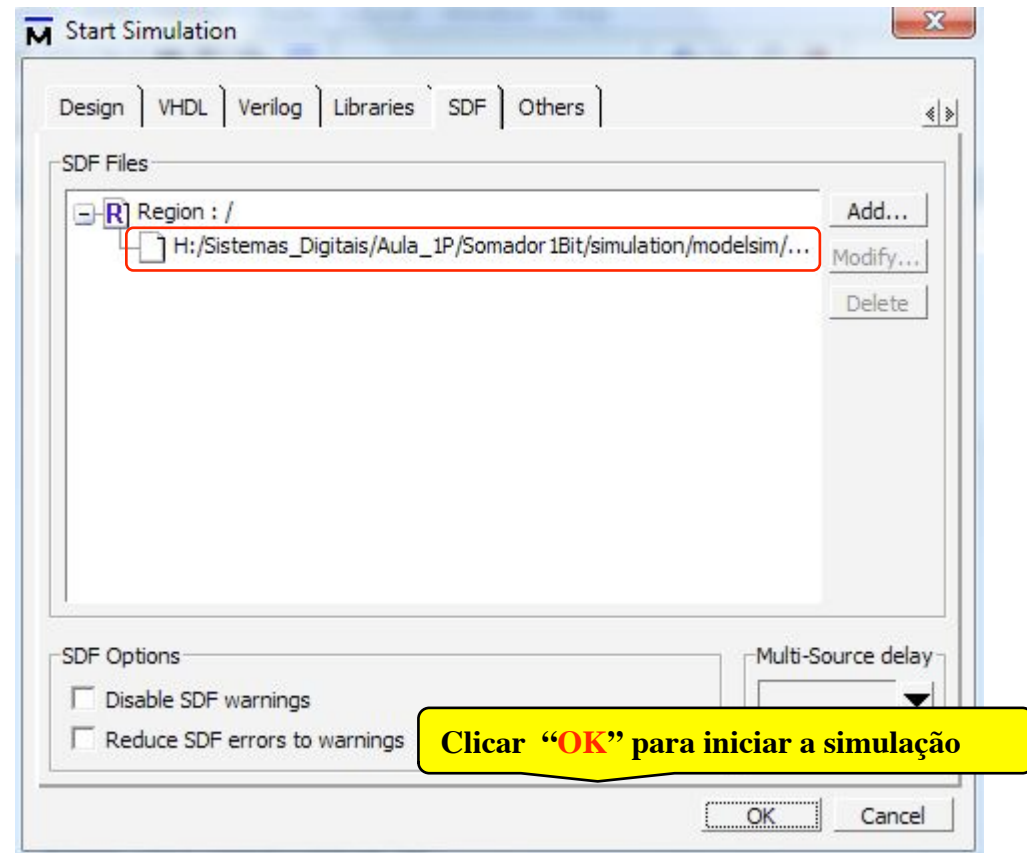
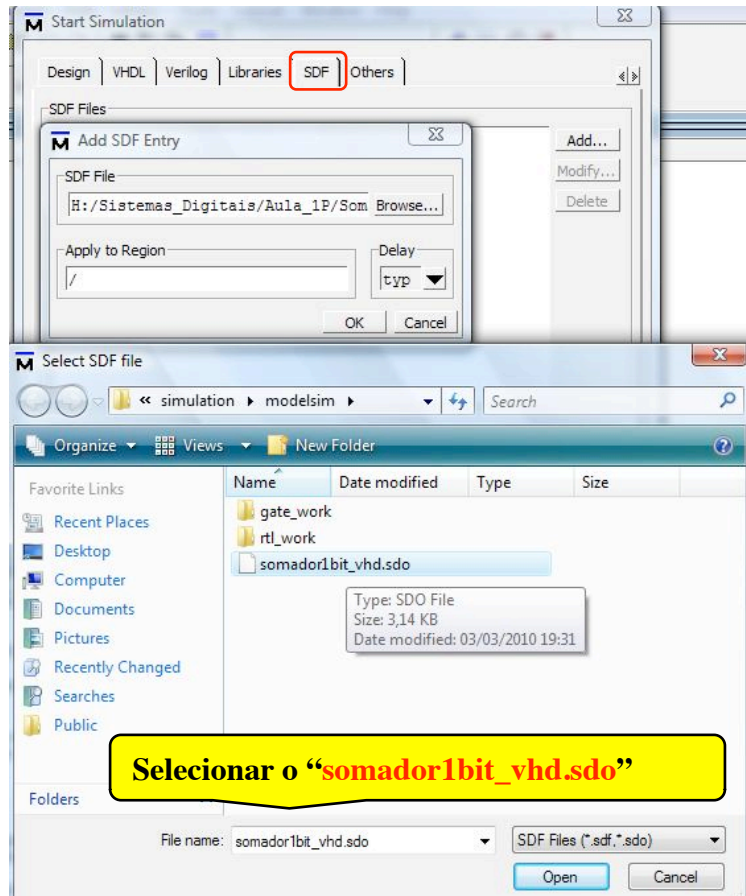
The image shows the ModelSim ALTERA STARTER EDITION 6.5b interface. The 'Start Simulation' dialog box is open, with the 'SDF' tab selected. The 'Name' list contains the following entries:

Name	Type	Path
work	Library	H:/Sistemas_Digitais/Aula_1P/Somador1Bit/simulation/modelsim/gate_wor
gate_work	Library	H:/Sistemas_Digitais/Aula_1P/Somador1Bit/simulation/modelsim/rti_work
rti_work	Library	H:/Sistemas_Digitais/Aula_1P/Somador1Bit/simulation/modelsim/rti_work
220model	Library	\$MODEL_TECH/./altera/vhdl/220model
220model_ver	Library	\$MODEL_TECH/./altera/verilog/220model
altera	Library	\$MODEL_TECH/./altera/vhdl/altera
altera_mf	Library	\$MODEL_TECH/./altera/vhdl/altera_mf
altera_mf_ver	Library	\$MODEL_TECH/./altera/verilog/altera_mf
altera_ver	Library	\$MODEL_TECH/./altera/verilog/altera
altgxb	Library	\$MODEL_TECH/./altera/vhdl/altgxb
altgxb_lib	Library	\$MODEL_TECH/./altera/vhdl/altgxb
altgxb_ver	Library	\$MODEL_TECH/./altera/verilog/altgxb
arriagx	Library	\$MODEL_TECH/./altera/vhdl/arriagx
arriagx_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriagx_hssi
arriagx_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriagx_hssi
arriagx_ver	Library	\$MODEL_TECH/./altera/verilog/arriagx
arriaii	Library	\$MODEL_TECH/./altera/vhdl/arriaii
arriaii_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriaii_hssi

The 'Design Unit(s)' field is set to 'work.somador1bit' and the 'Resolution' is set to 'default'. The 'Optimization' checkbox is unchecked. The 'OK' button is highlighted.

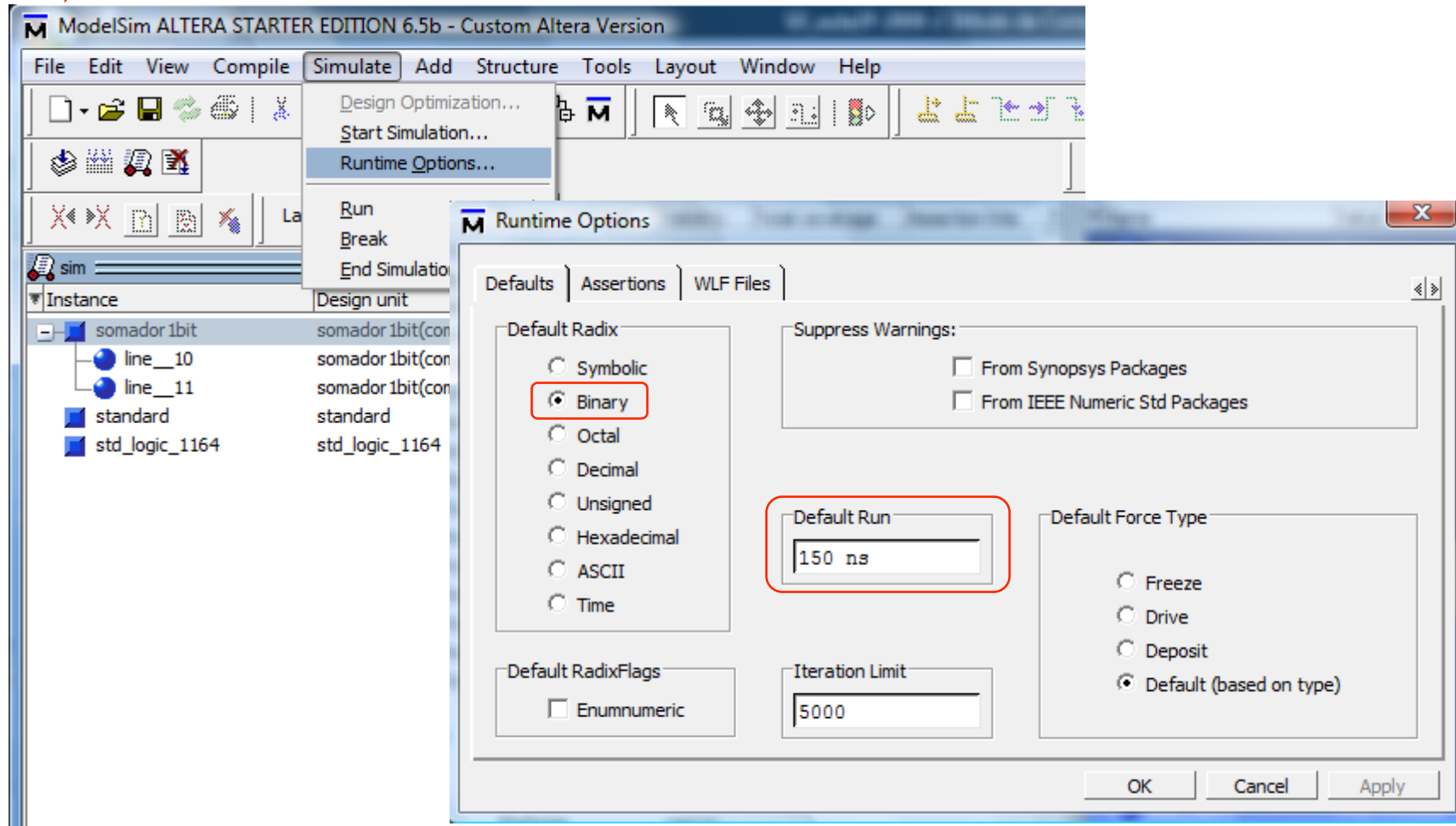
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▶ Iniciar simulação “Gate-Level”



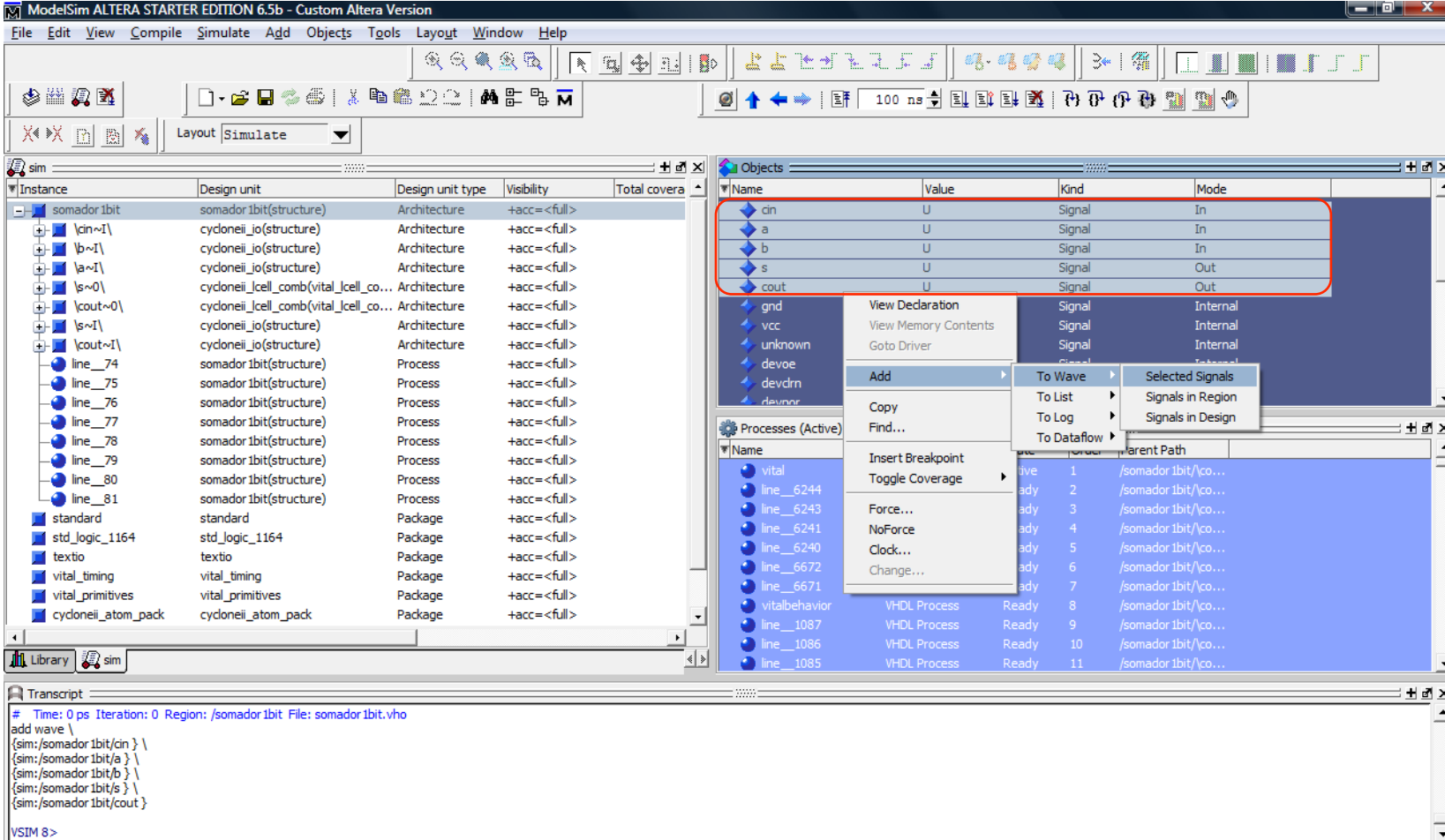
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▶ Alterar opções de simulação



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▶ Adicionar os sinais às “waveforms”



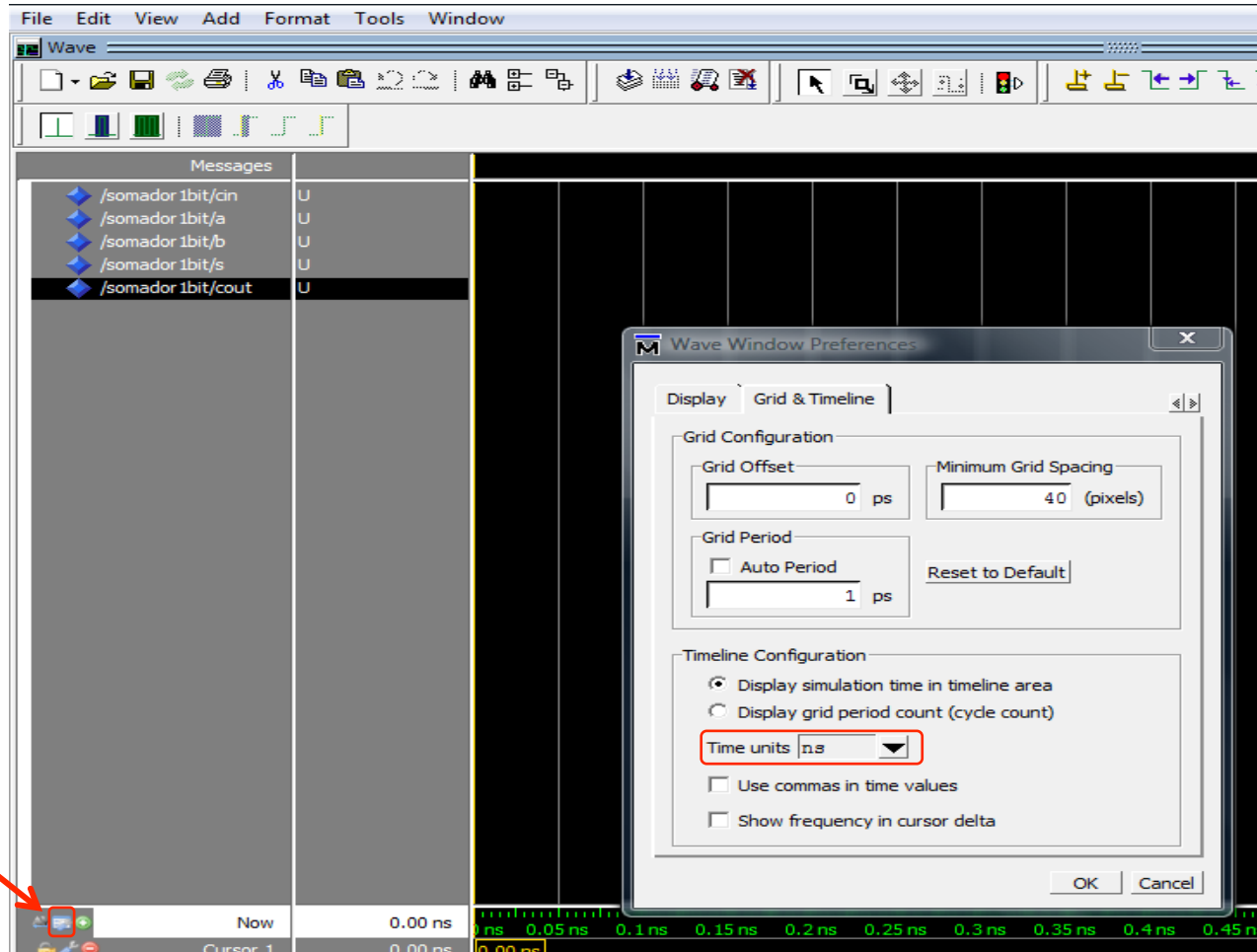
The screenshot shows the ModelSim ALTERA STARTER EDITION 6.5b interface. The 'Objects' window is open, displaying a list of signals and processes. A context menu is open over the signal list, with the 'Add' option selected, and the 'To Wave' submenu is also open, showing 'Selected Signals' as the chosen option. The 'Transcript' window at the bottom shows the commands used to add the signals to the waveform.

Name	Value	Kind	Mode
cin	U	Signal	In
a	U	Signal	In
b	U	Signal	In
s	U	Signal	Out
cout	U	Signal	Out
gnd		Signal	Internal
vcc		Signal	Internal
unknown		Signal	Internal
devoe		Signal	Internal
devdrn		Signal	Internal
devvnr		Signal	Internal

```
# Time: 0 ps Iteration: 0 Region: /somador1bit File: somador1bit.vho
add wave \
{sim:/somador1bit/cin} \
{sim:/somador1bit/a} \
{sim:/somador1bit/b} \
{sim:/somador1bit/s} \
{sim:/somador1bit/cout}
VSIM 8>
```

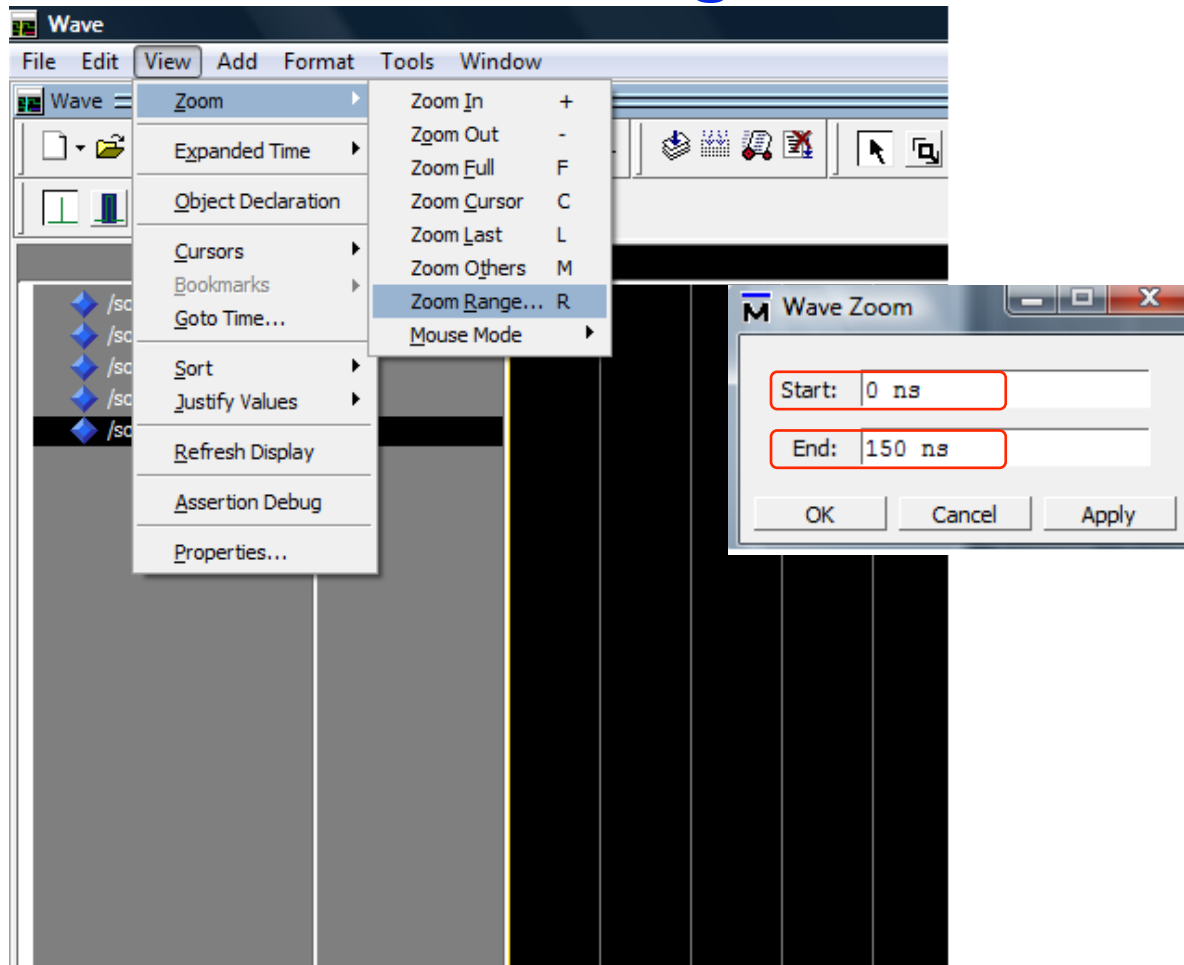
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▶ Alterar a unidade de tempo das “waveforms”



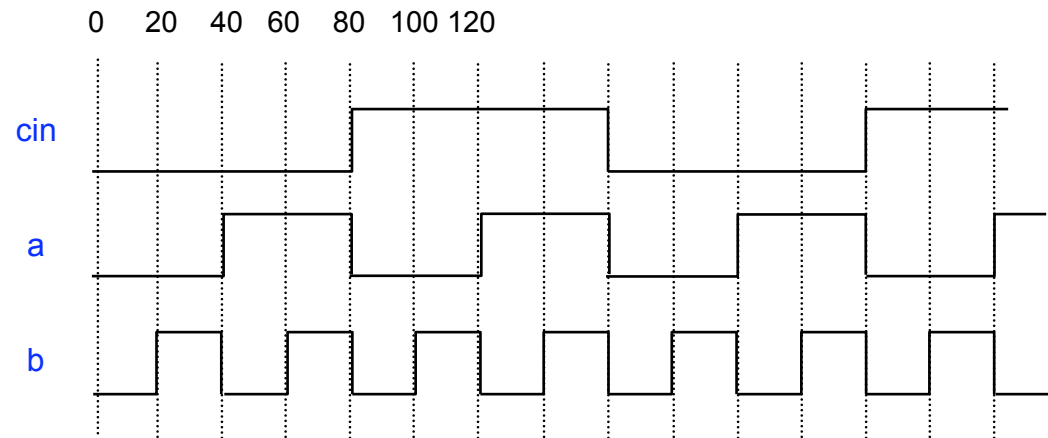
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▶ Alterar o “zoom range” das “waveforms”



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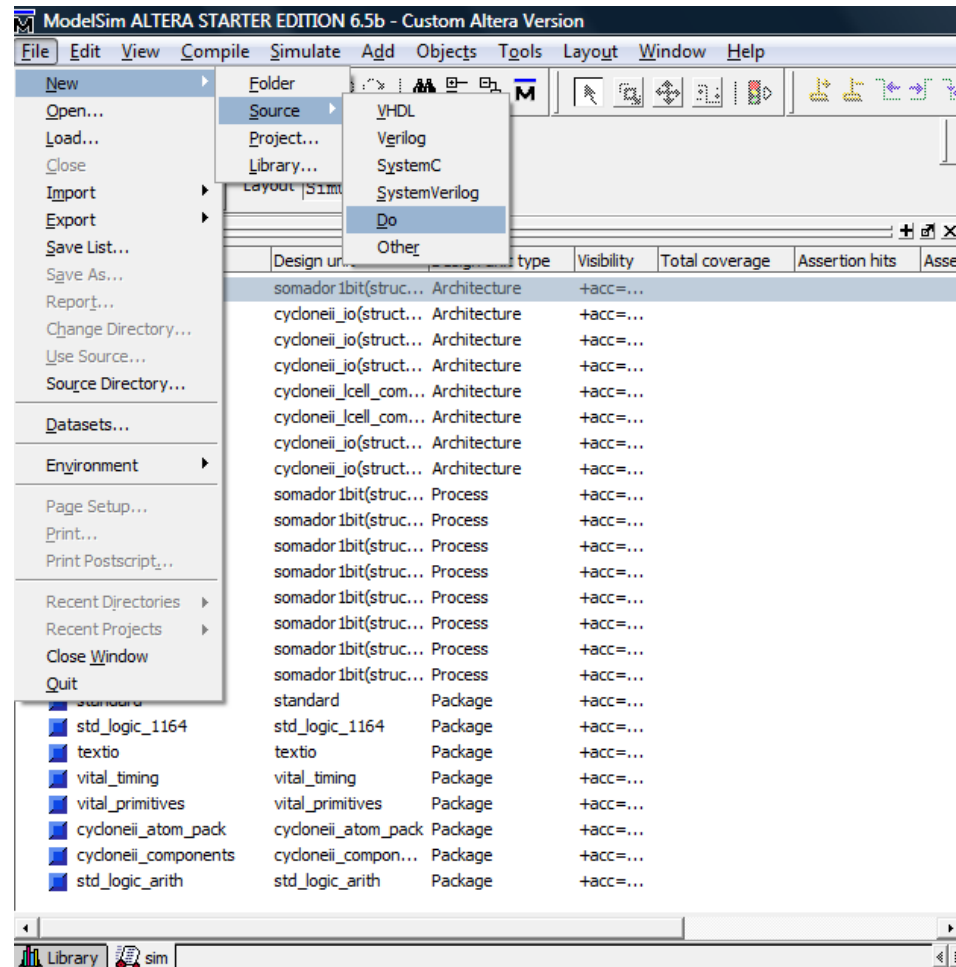
▶ Arquivo de estímulos de entrada



```
#força a entrada cin para 0 no tempo 0 ns
#força cin para 1 no tempo 80 ns, repete a cada 160 ns
force /cin 0 0 ns, 1 80 ns -r 160 ns
force /a 0 0 ns, 1 40 ns -r 80 ns
force /b 0 0 ns, 1 20 ns -r 40 ns
```

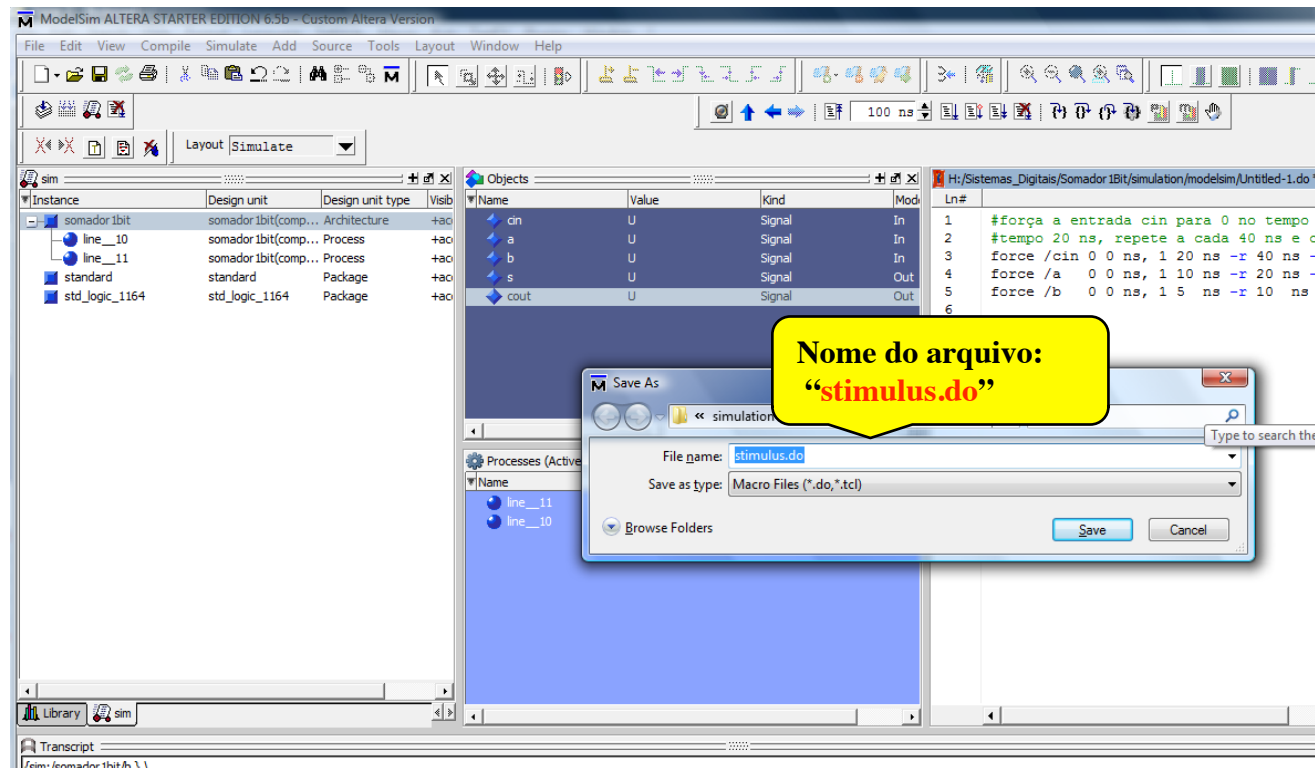
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▶ Criar novo arquivo de estímulos de entrada



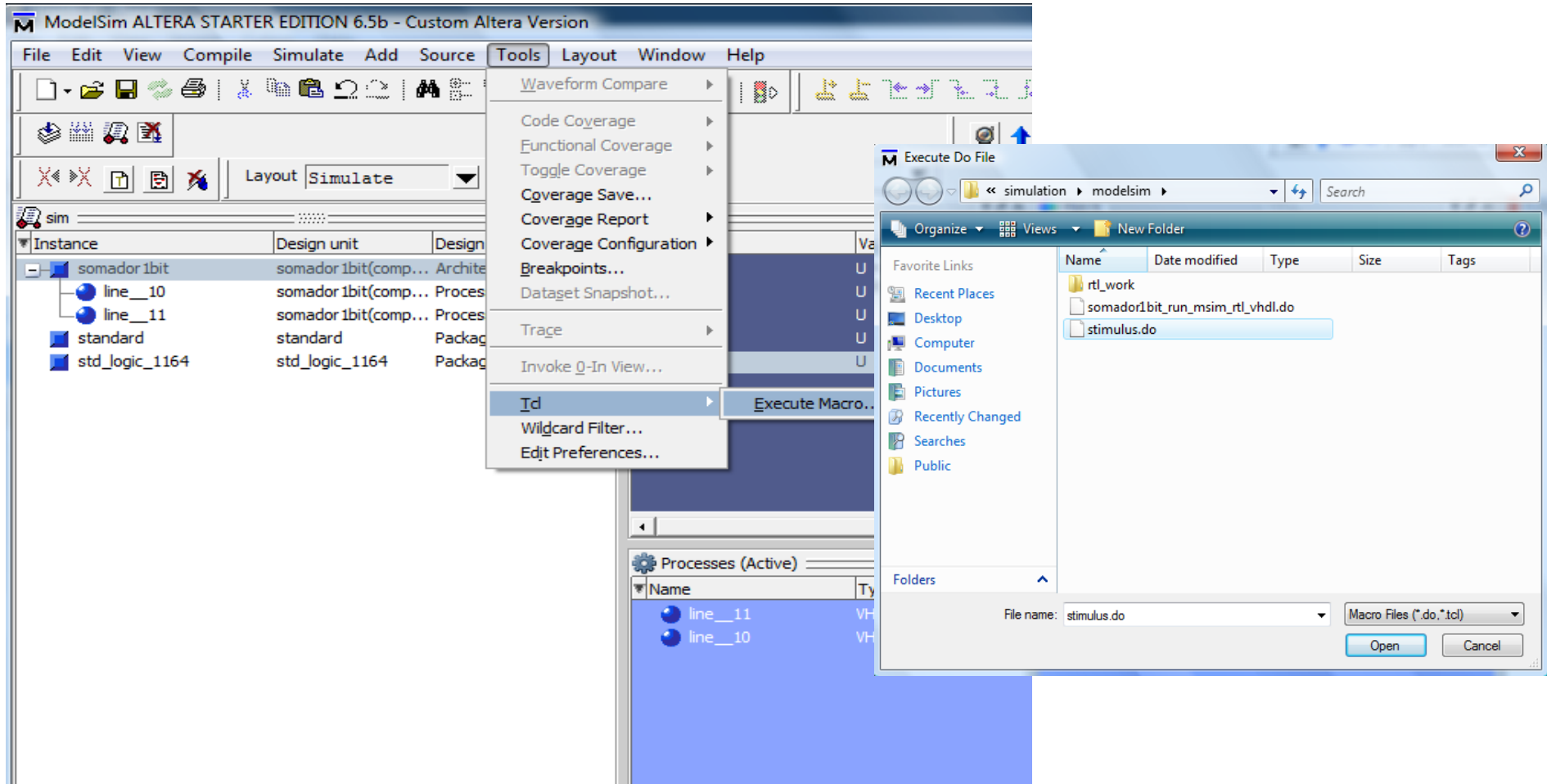
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▶ Salvar arquivo de estímulos de entrada



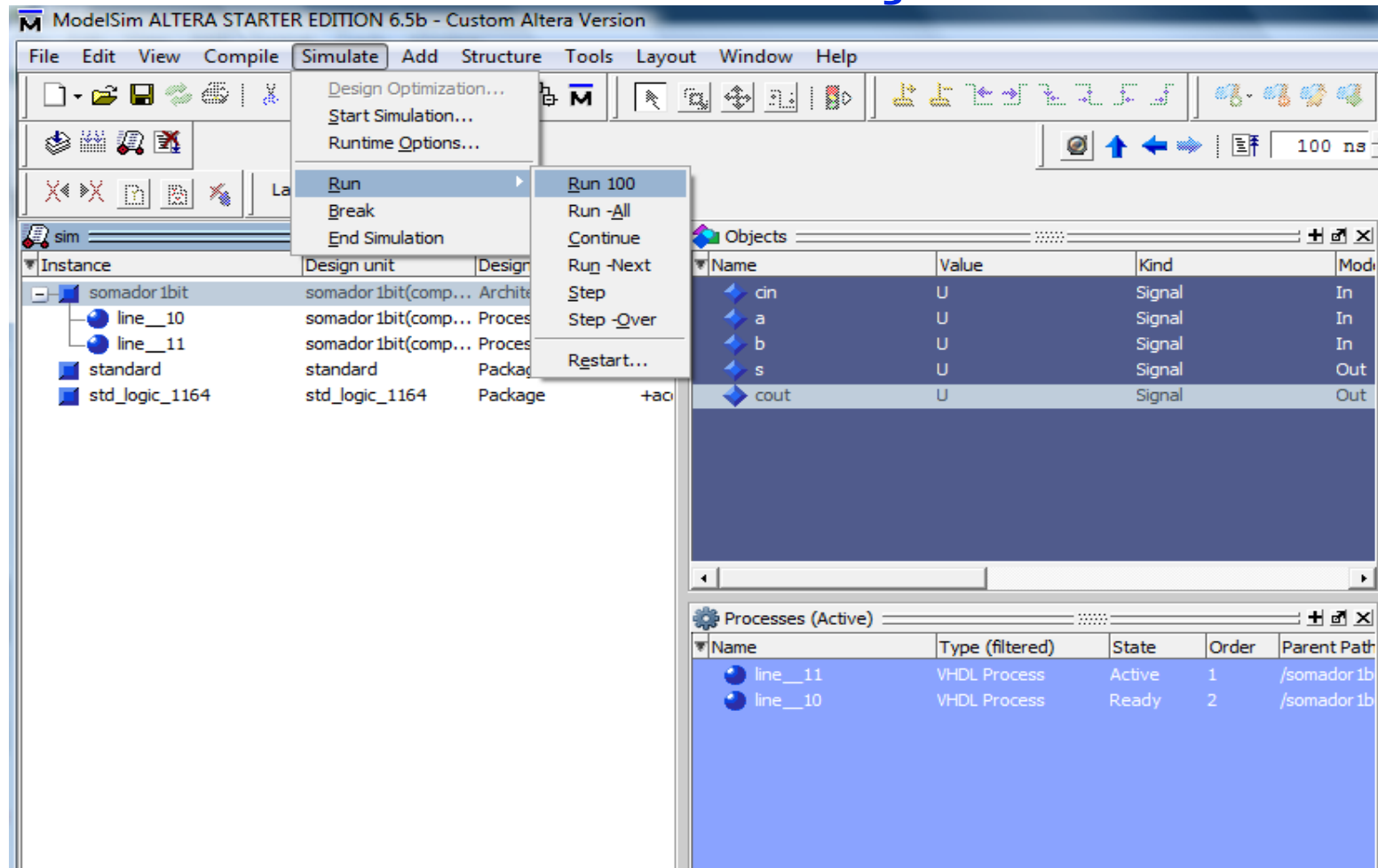
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▶ Executar arquivo de estímulos de entrada



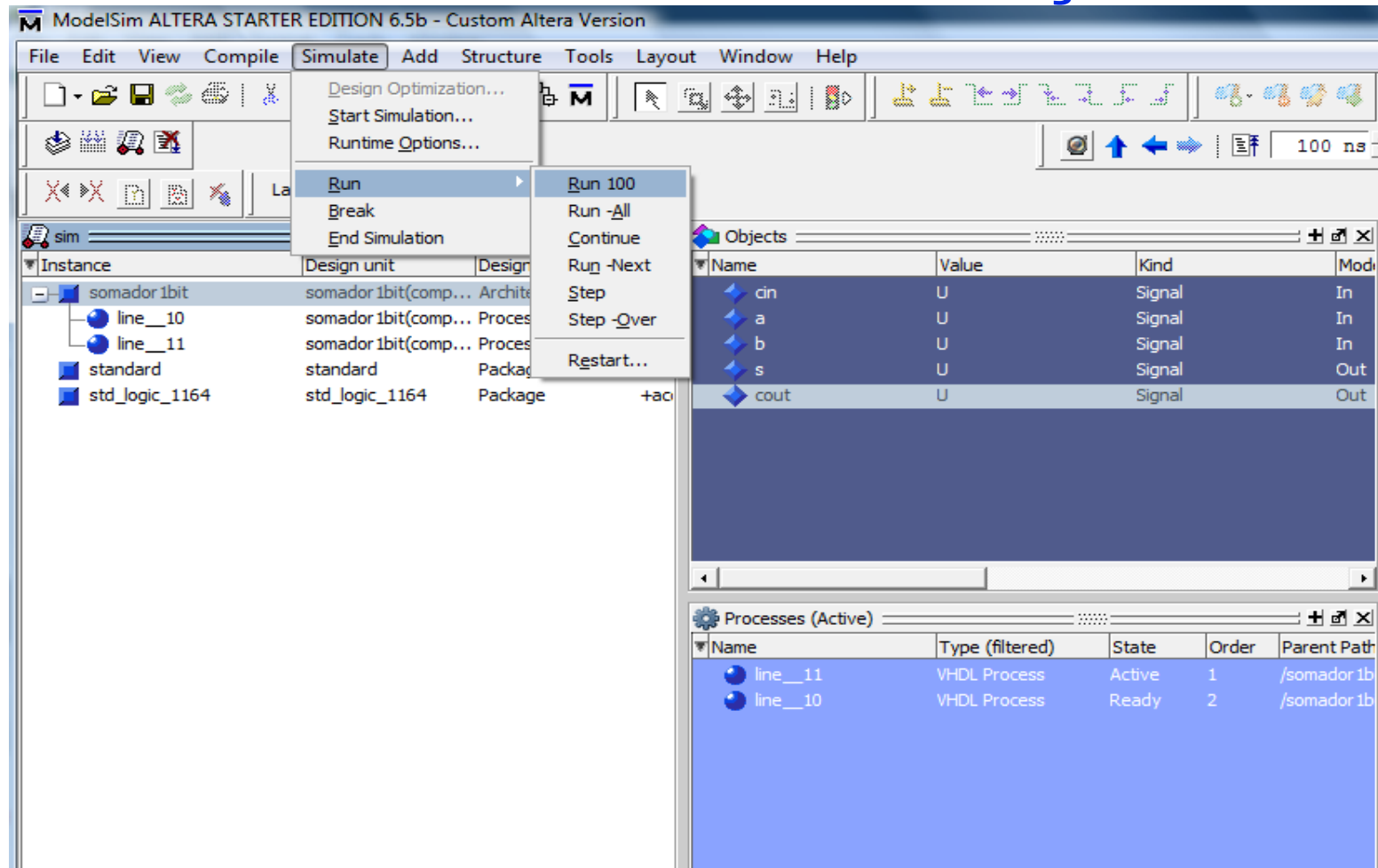
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▶ Executar 100ns de simulação



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▶ Executar mais 100ns de simulação



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▶ Analisar os resultados da simulação



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▶ Reiniciar a simulação

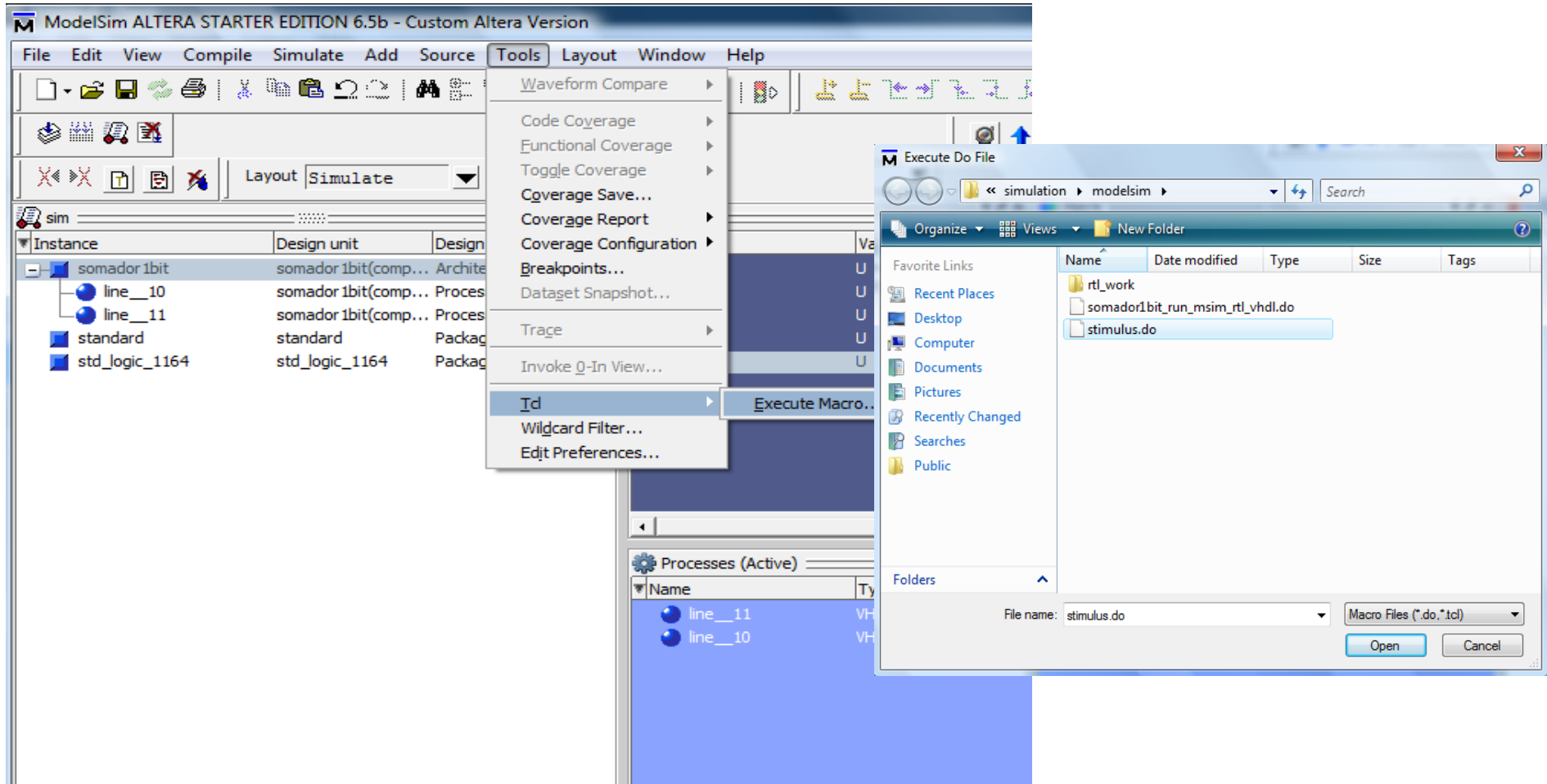
The screenshot shows the ModelSim ALTERA STARTER EDITION 6.5b interface. The main window displays a simulation table with columns for Instance, Design unit, Design unit type, and Visibility. A 'Restart' dialog box is open, showing a 'Keep:' section with several checked options: List Format, Wave Format, Breakpoints, Logged Signals, Virtual Definitions, Assertions, Cover Directives, and ATV Format. The 'OK' button is highlighted with a red box, and a red arrow points to the 'Restart' button in the toolbar.

Instance	Design unit	Design unit type	Visibility
- somador 1bit	somador 1bit(structure)	Architecture	+acc=<fu
+ \cin~I\	cydoneii_io(structure)	Architecture	+acc=<fu
+ \b~I\	cydoneii_io(structure)	Architecture	+acc=<fu
+ \a~I\	cydoneii_io(structure)	Architecture	+acc=<fu
+ \s~0\	cydoneii_1cell_comb(vital_1cell_co...	Architecture	+acc=<fu
+ \cout~0\	cydoneii_1cell_comb(vital_1cell_co...	Architecture	+acc=<fu
+ \s~1\	cydoneii_io(structure)	Architecture	+acc=<fu
+ \cout~1\	cydoneii_io(structure)	Architecture	+acc=<fu
line__74	somador 1bit(structure)	Process	+acc=<fu
line__75	somador 1bit(structure)	Process	+acc=<fu
line__76	somador 1bit(structure)	Process	+acc=<fu

Keep:	Value
<input checked="" type="checkbox"/> List Format	1
<input checked="" type="checkbox"/> Wave Format	0
<input checked="" type="checkbox"/> Breakpoints	0
<input checked="" type="checkbox"/> Logged Signals	1
<input checked="" type="checkbox"/> Virtual Definitions	0
<input checked="" type="checkbox"/> Assertions	1
<input checked="" type="checkbox"/> Cover Directives	X
<input checked="" type="checkbox"/> ATV Format	1

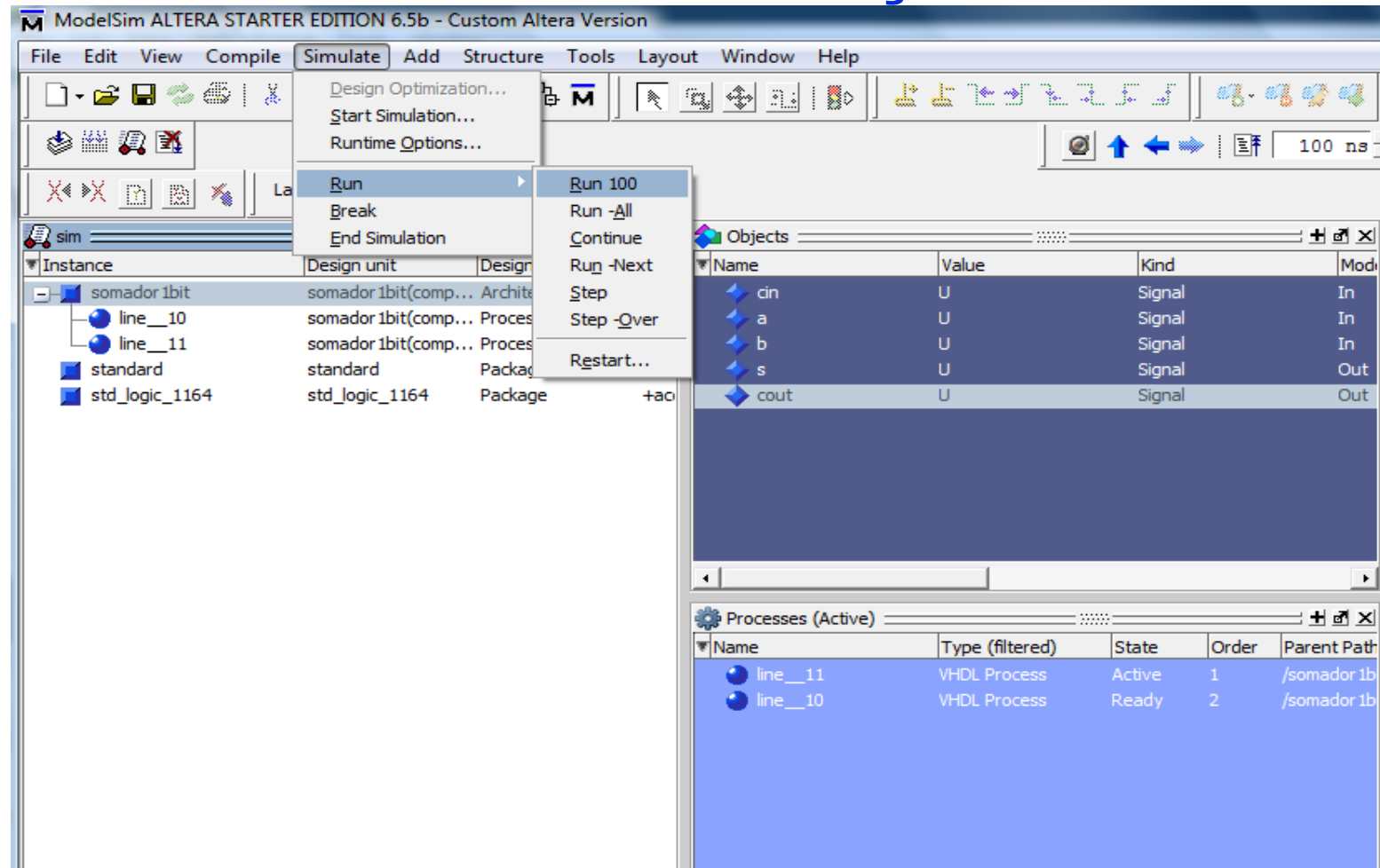
Projeto de Sistemas Digitais com Ferramentas EDA

▶ Executar arquivo de estímulos de entrada



Projeto de Sistemas Digitais com Ferramentas EDA

▶ Executar 100ns de simulação



Projeto de Sistemas Digitais com Ferramentas EDA

▶ Analisar os resultados da simulação

