Digital Integrated Circuits
A Design Perspective

Semiconductor Memories
(Part 1)

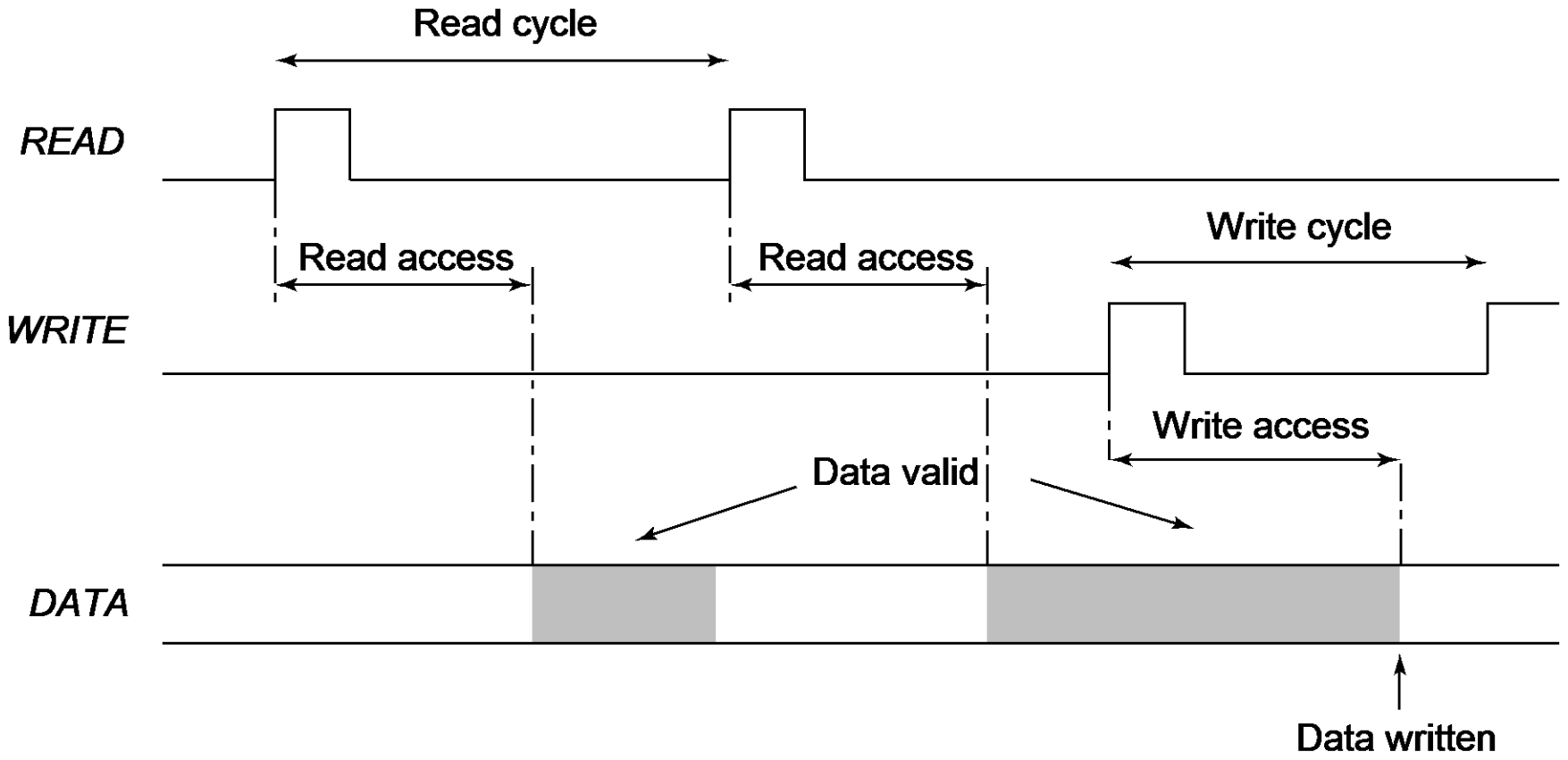
Reference: Digital Integrated Circuits, 2nd edition, Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic

Disclaimer: slides adapted for INE5442/EEL7312 by José L. Güntzel and Luiz dos Santos from the book´s companion slides made available by the authors.

Lecture Summary

- Memory Classification
- Memory Architectures
- The Memory Core (ROM Memories)

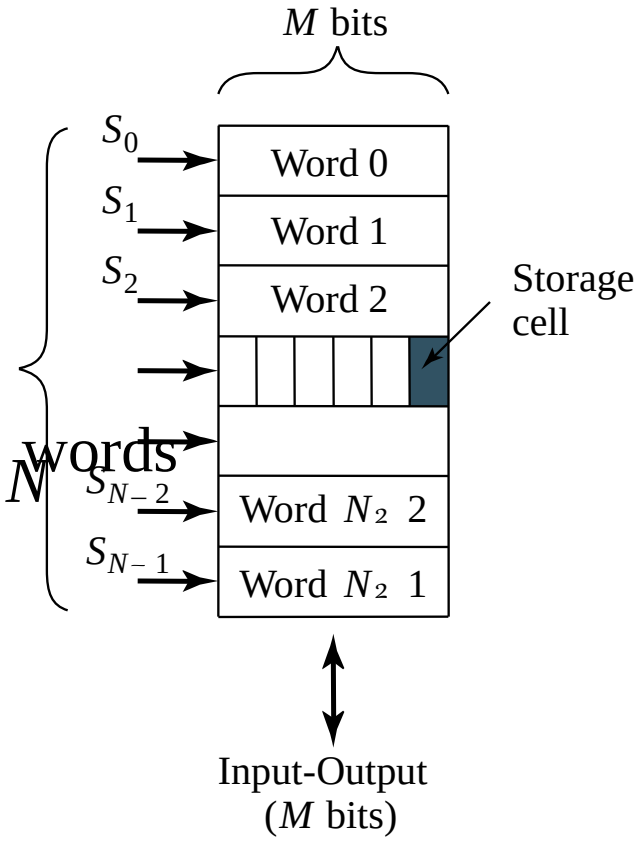
Memory Timing: Definitions



Semiconductor Memory Classification

Read-Write Memory		Non-Volatile Read-Write Memory	Read-Only Memory
Random Access	**Non-Random Access**	EPROM E^2PROM FLASH	Mask-Programmed Programmable (PROM)
SRAM DRAM	FIFO LIFO Shift Register CAM		

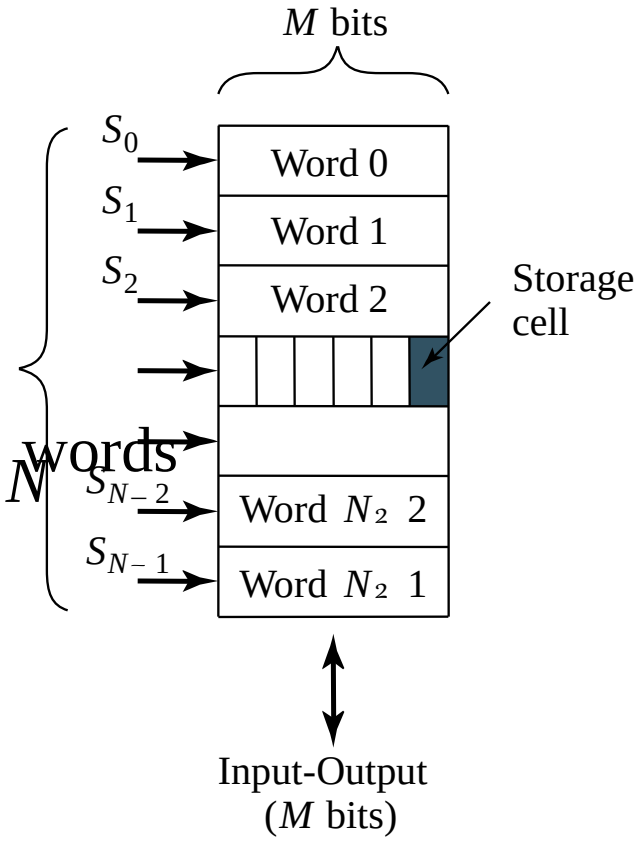
Memory Architecture: Decoders

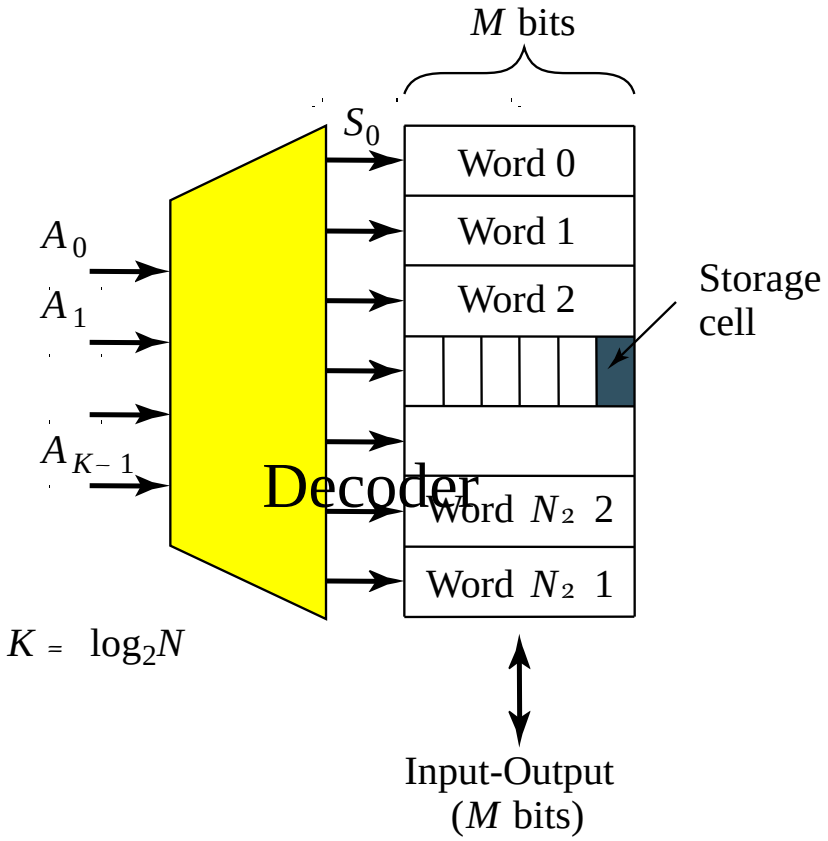


Decoder

Intuitive architecture for N x M memory
Too many select signals:
N words == N select signals

Memory Architecture: Decoders





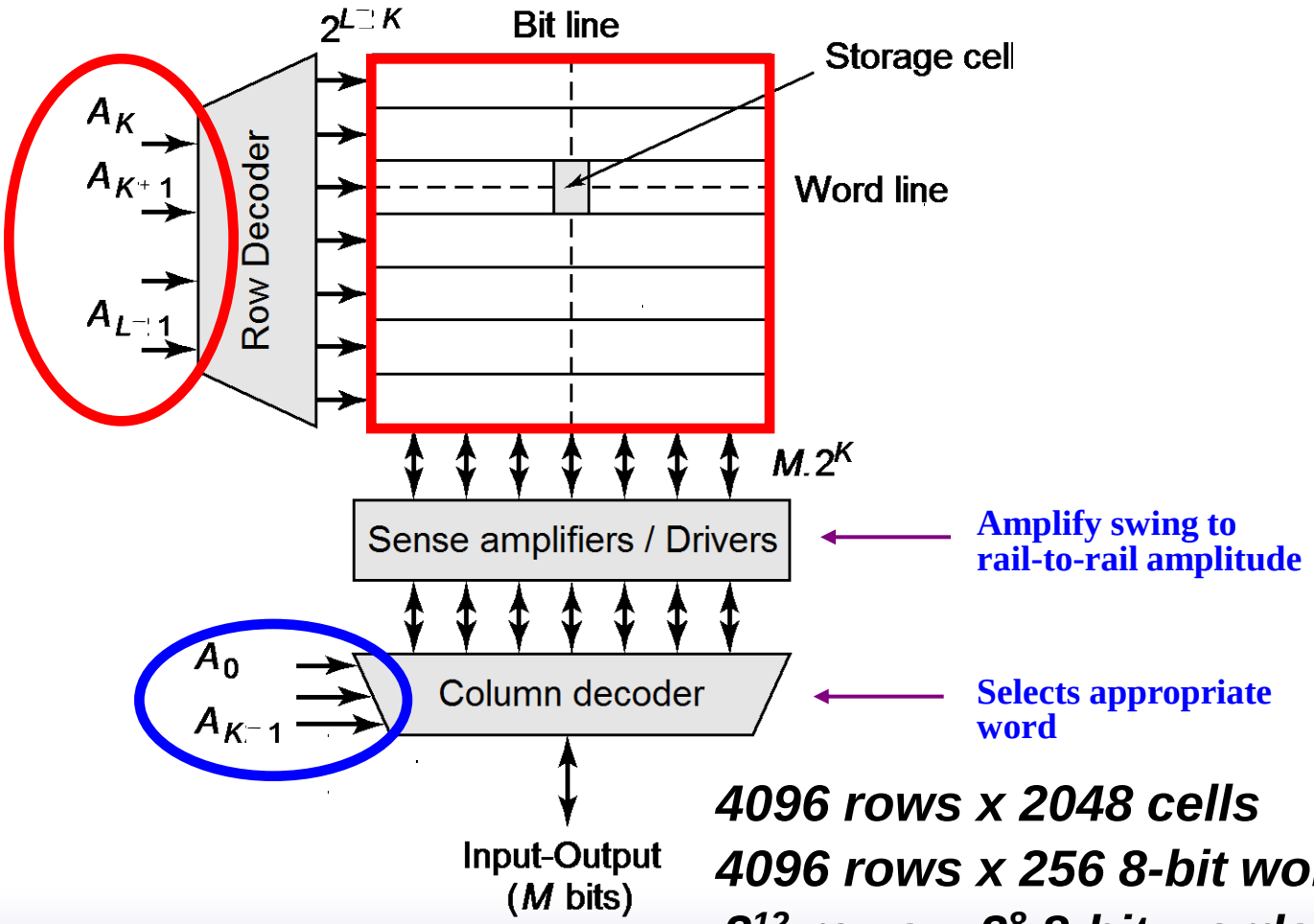
Intuitive architecture for N x M memory
Too many select signals:
N words == N select signals

Decoder reduces the number of select signals

$$K = log_2 N$$

Array-Structured Memory Architecture

Problem: ASPECT RATIO or HEIGHT >> WIDTH



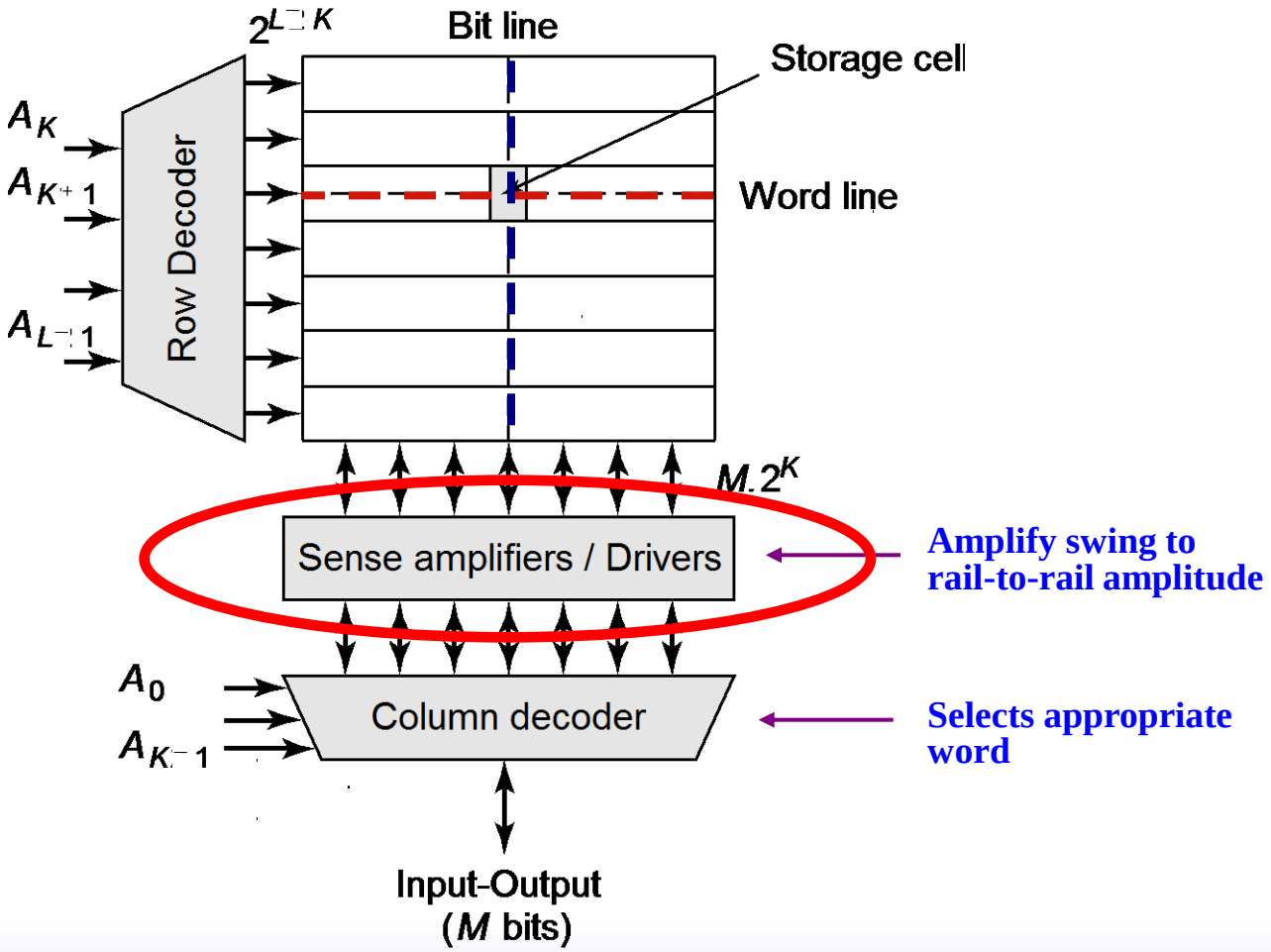
4096 rows x 2048 cells

4096 rows x 256 8-bit words

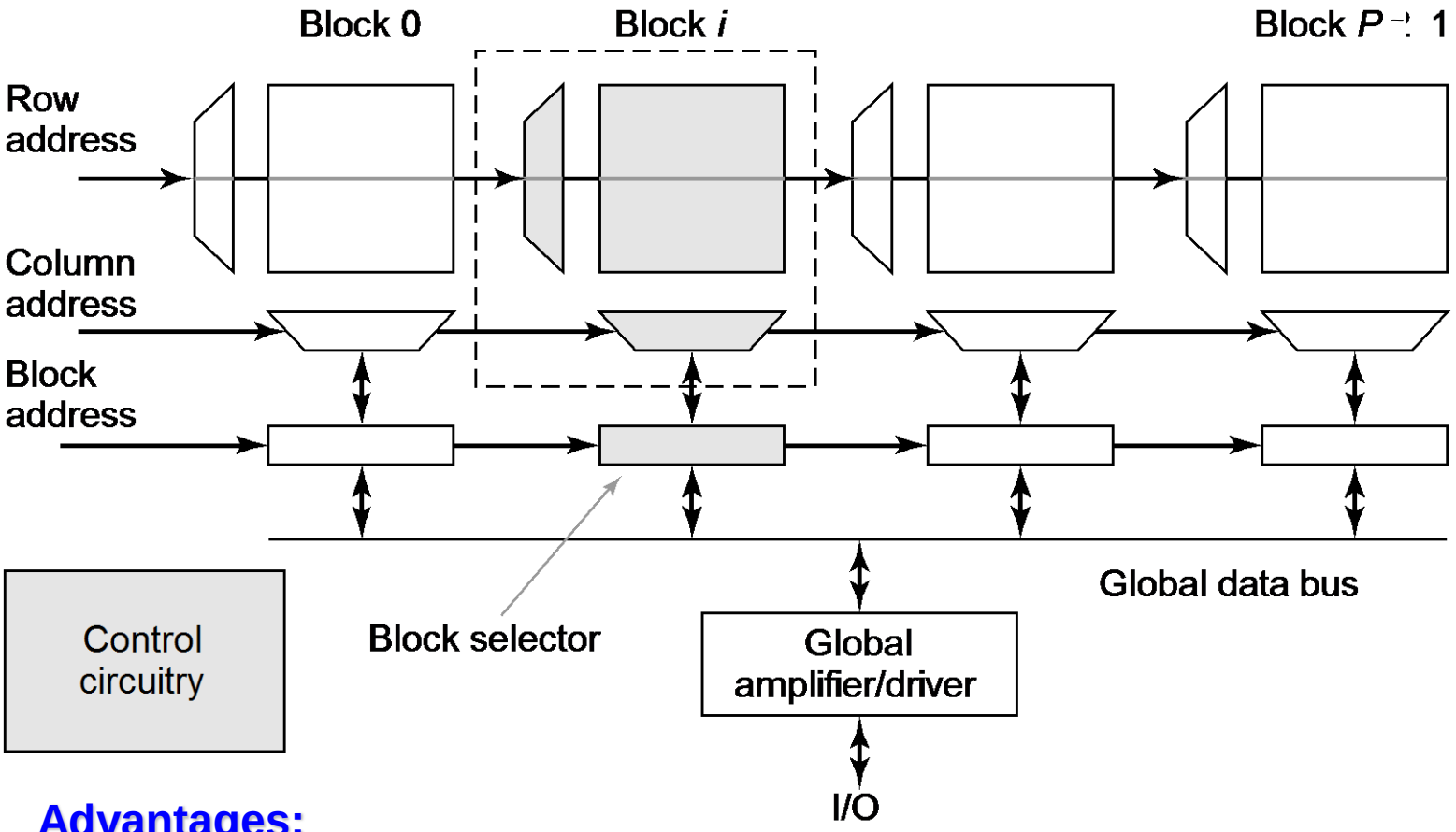
2^{12} rows x 2^8 8-bit words

Array-Structured Memory Architecture

Problem: ASPECT RATIO or HEIGHT >> WIDTH



Hierarchical Memory Architecture

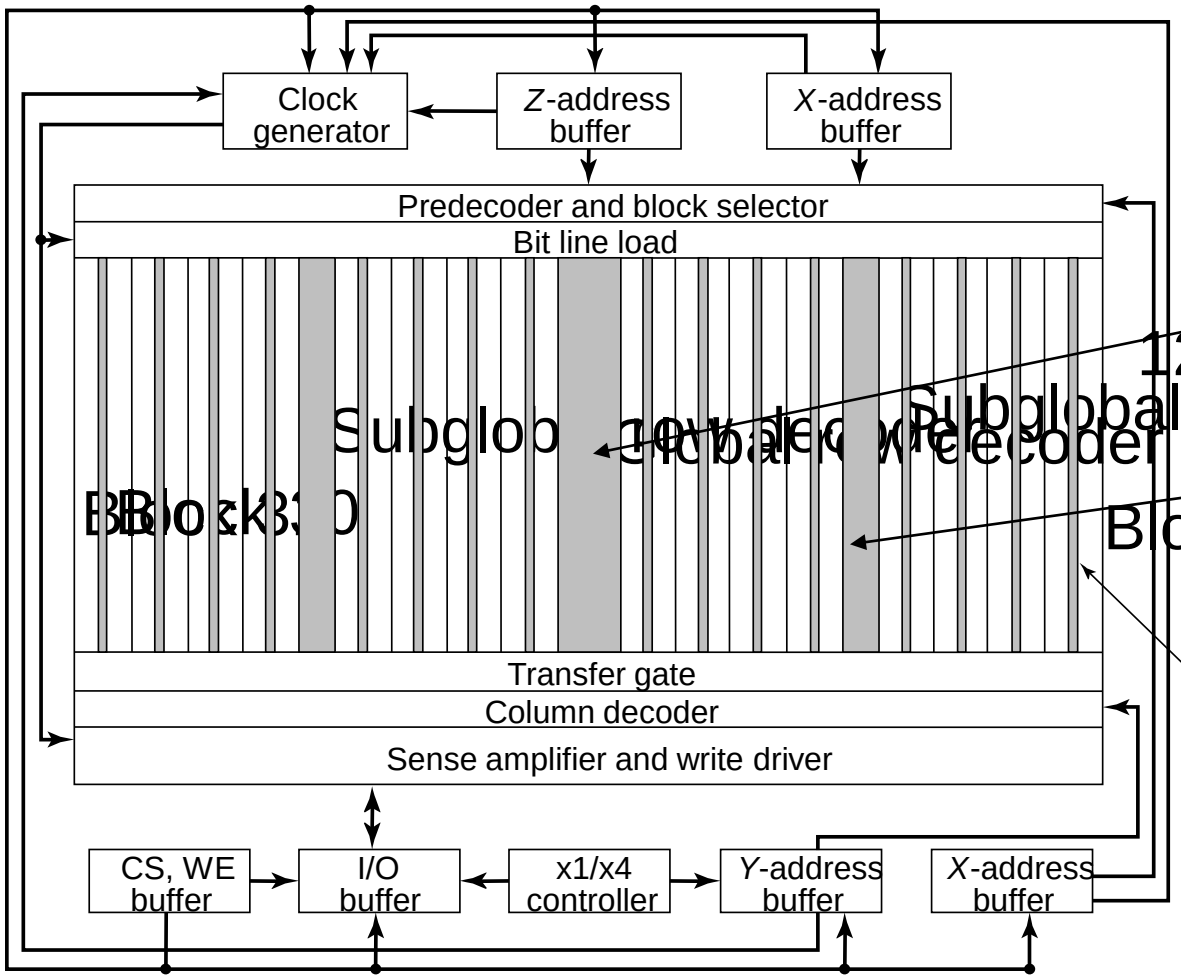


Advantages:

1. Shorter wires within blocks

2. Block address activates only 1 block => power savings

Block Diagram of 4 Mbit SRAM



32 128-bit blocks
(selected by a single row address)

Global row decoder

128 K Array Block

Subglobal row decoder

Sub-global row decoder

Block 1

Local row decoder

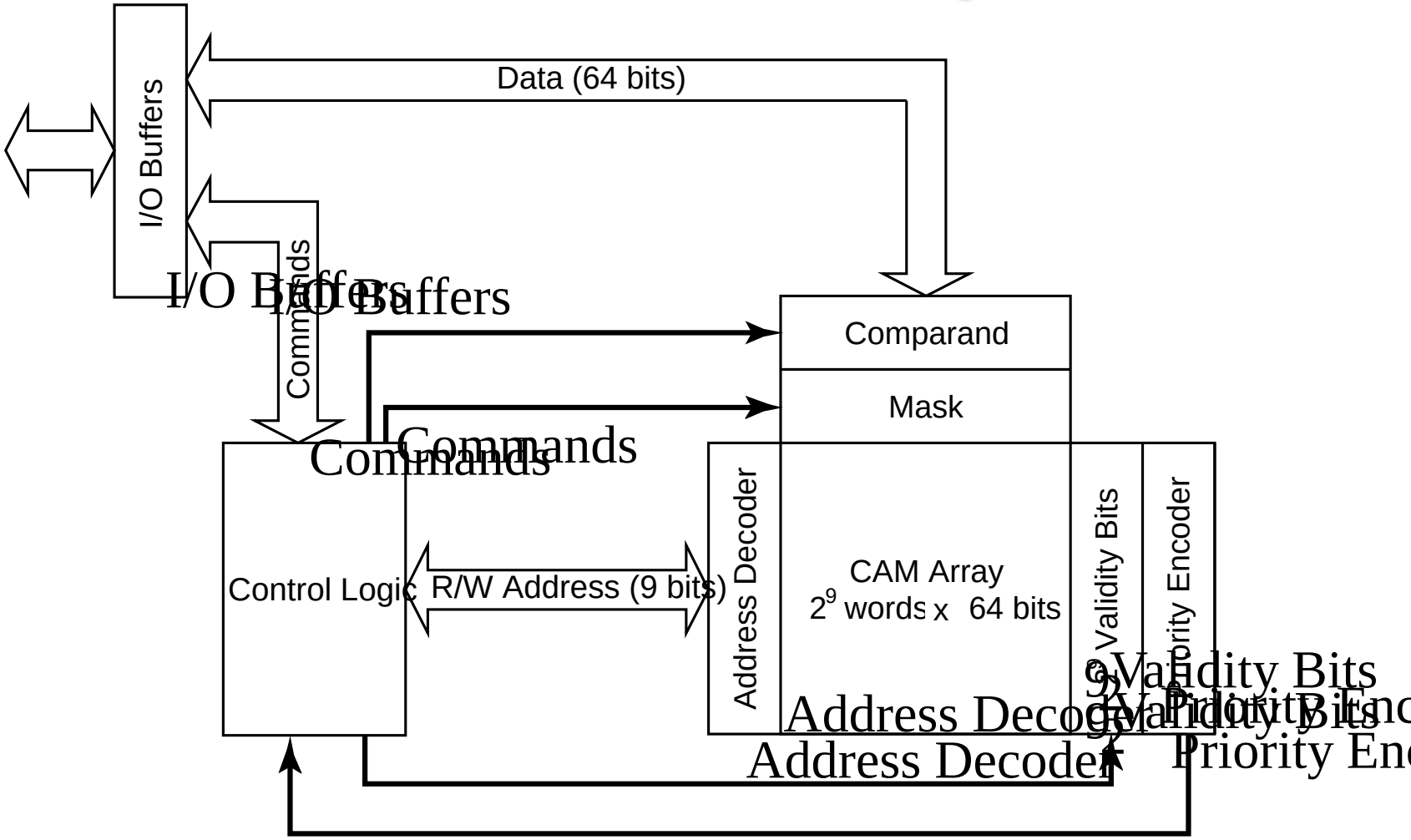
Local row dec

[Hirose90]

4Mbit = 32 blocks x 128Kbit = 32 blocks x 1024 rows x 128 columns

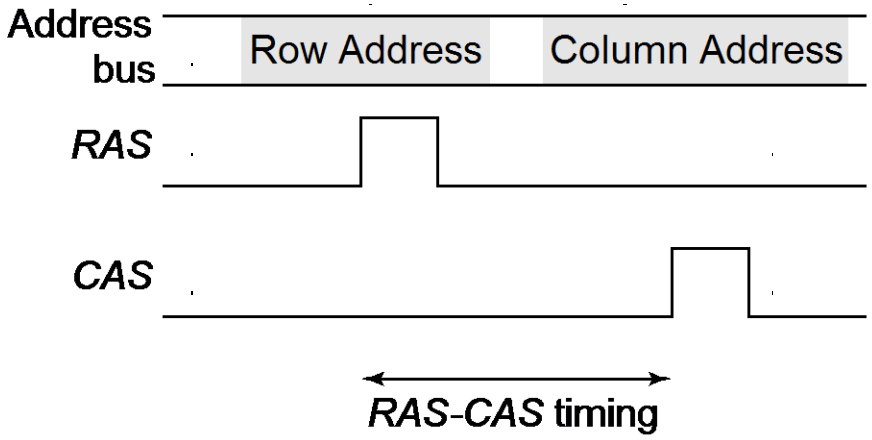
Z = 5, Y = 7, X = 10

Contents-Addressable Memory



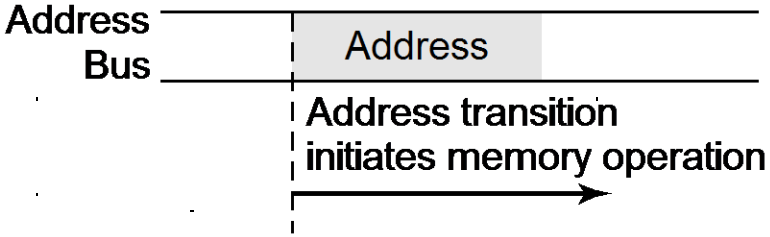
Memory Timing: Approaches

DRAM Timing
Multiplexed Addressing



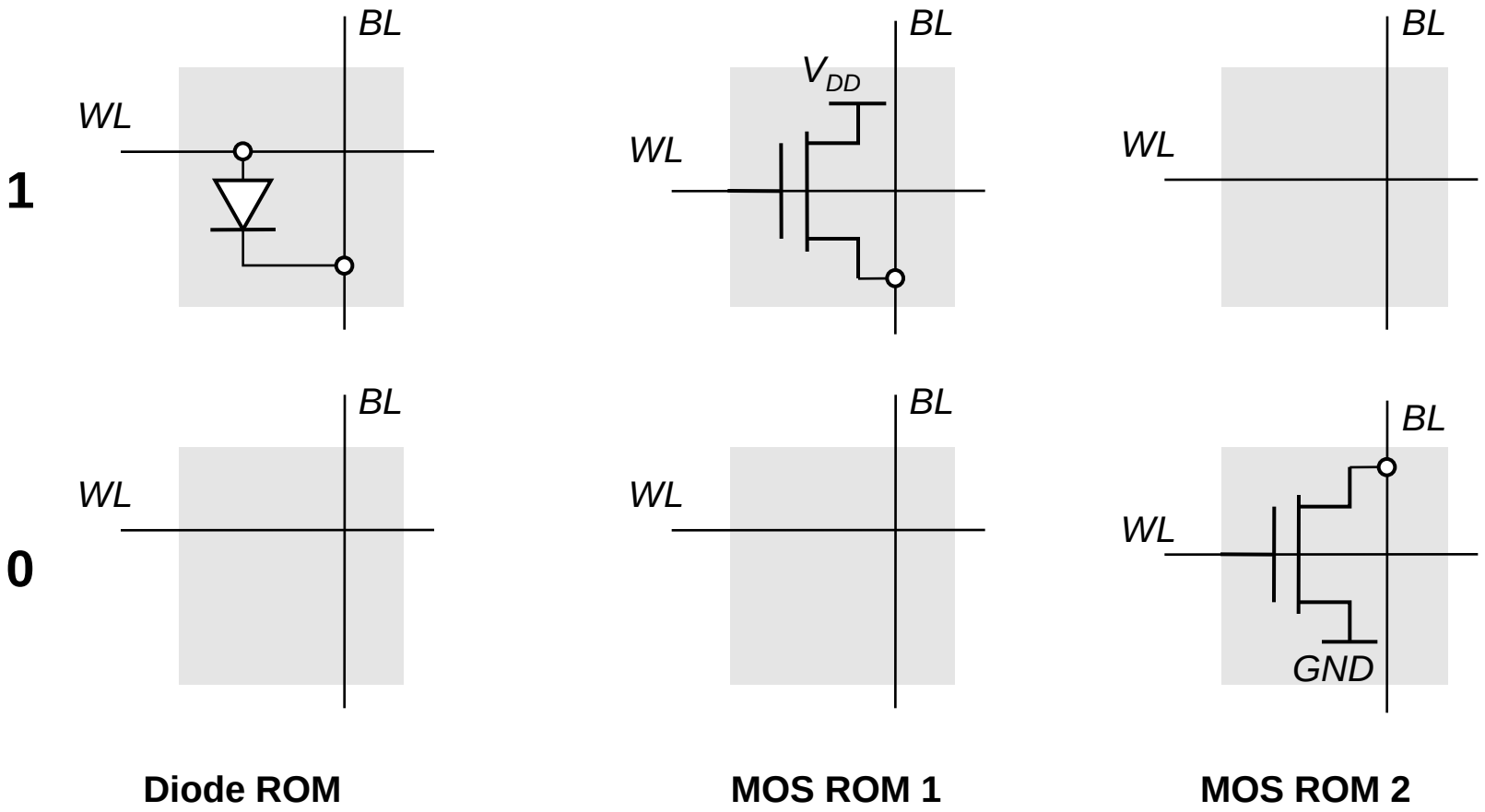
DRAM external timing signals:
RAS= Row Address Strobe
CAS=Column Address Strobe

SRAM Timing
Self-timed



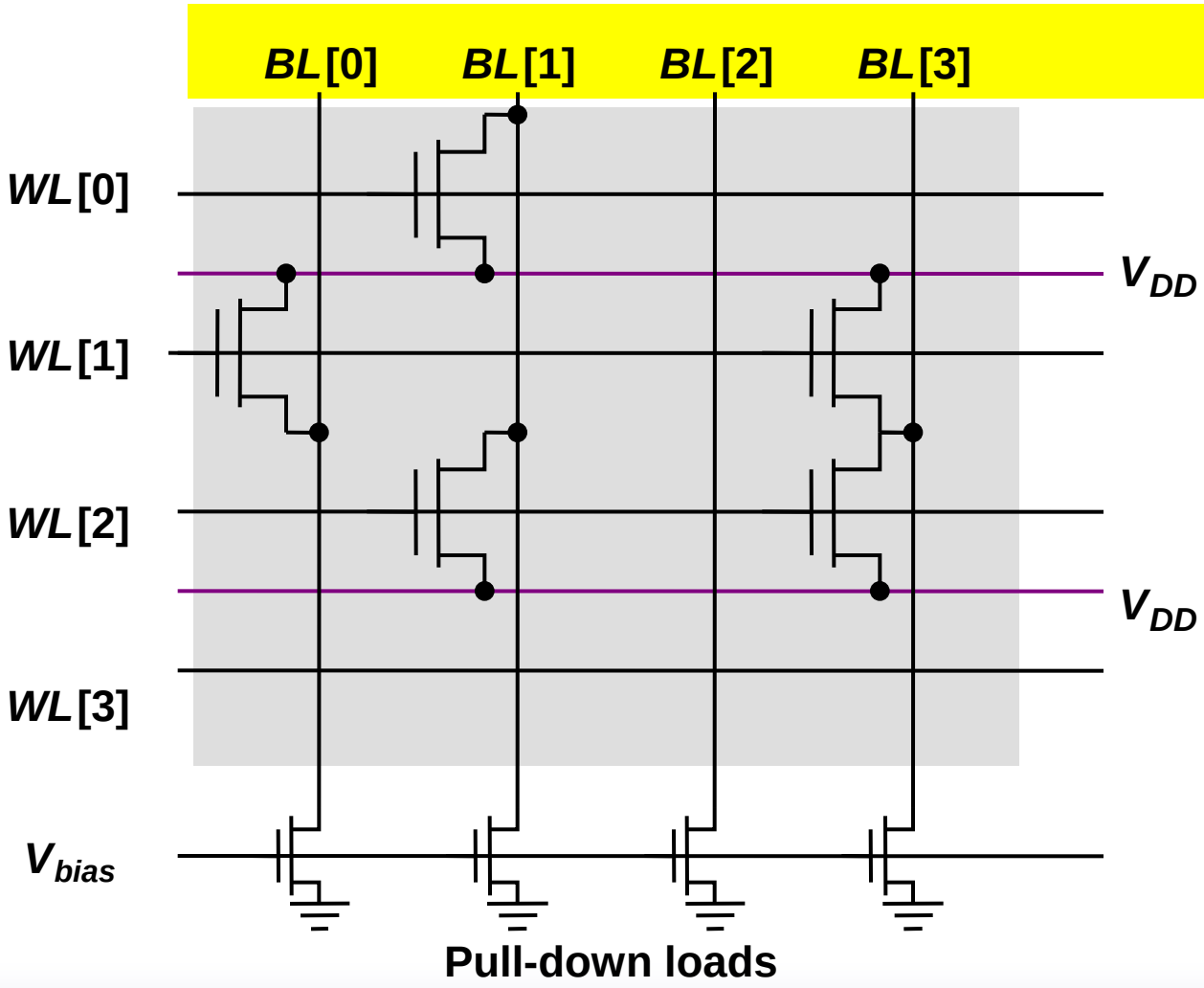
SRAM: no external timing signals!

Read-Only Memory Cells



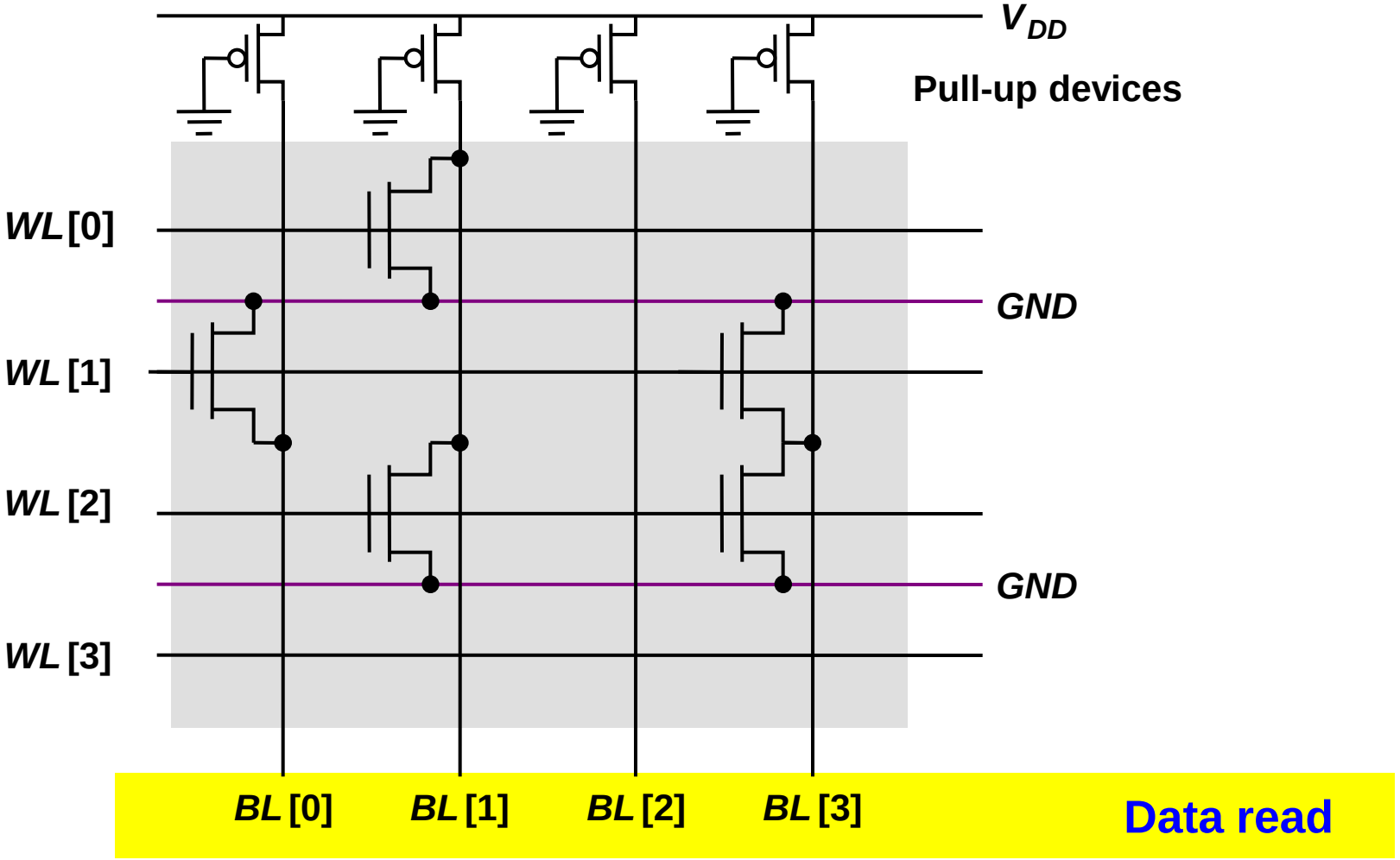
MOS ROM1: BL must be resistively clamped to ground
MOS ROM2: BL must be resistively clamped to Vdd

MOS OR ROM



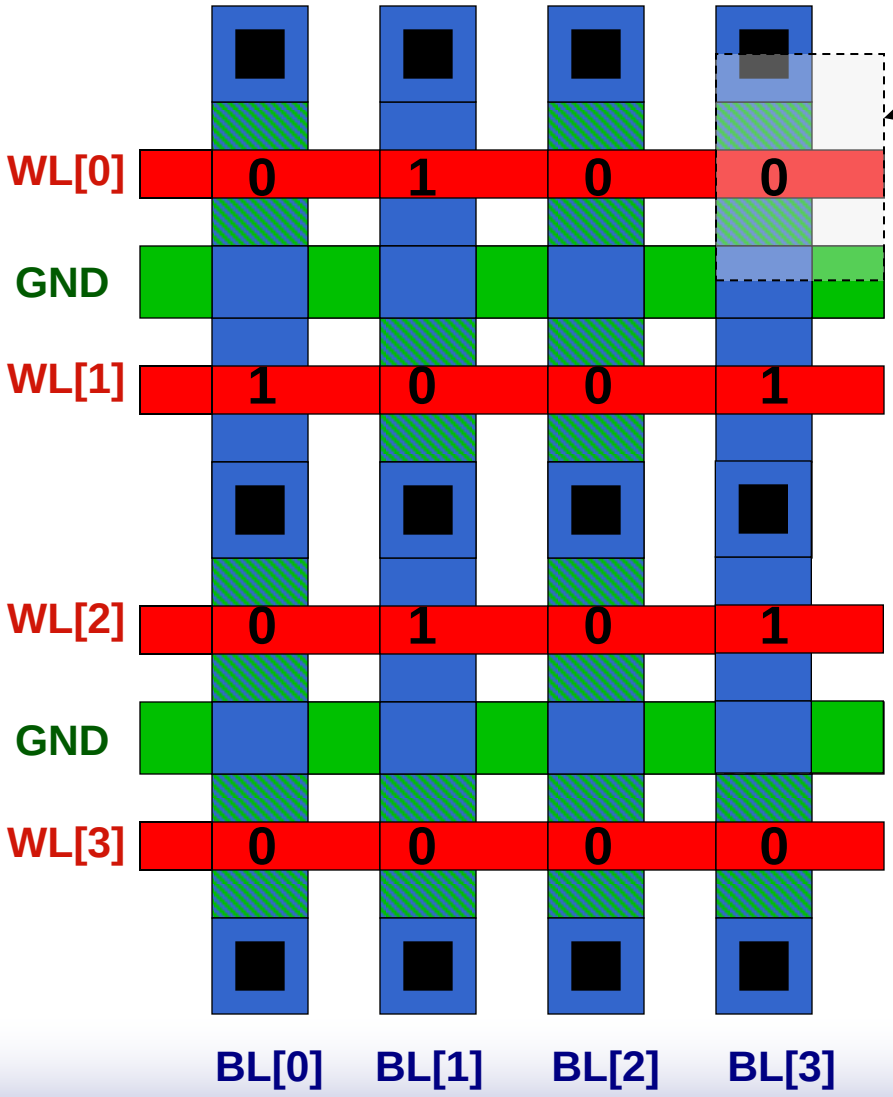
To reduce area overhead, supply voltage lines are shared between adjacent rows

MOS NOR ROM



Each column is a pseudo-NMOS (WLs are the inputs)!

MOS NOR ROM Layout



Programmming using the Active Layer Only

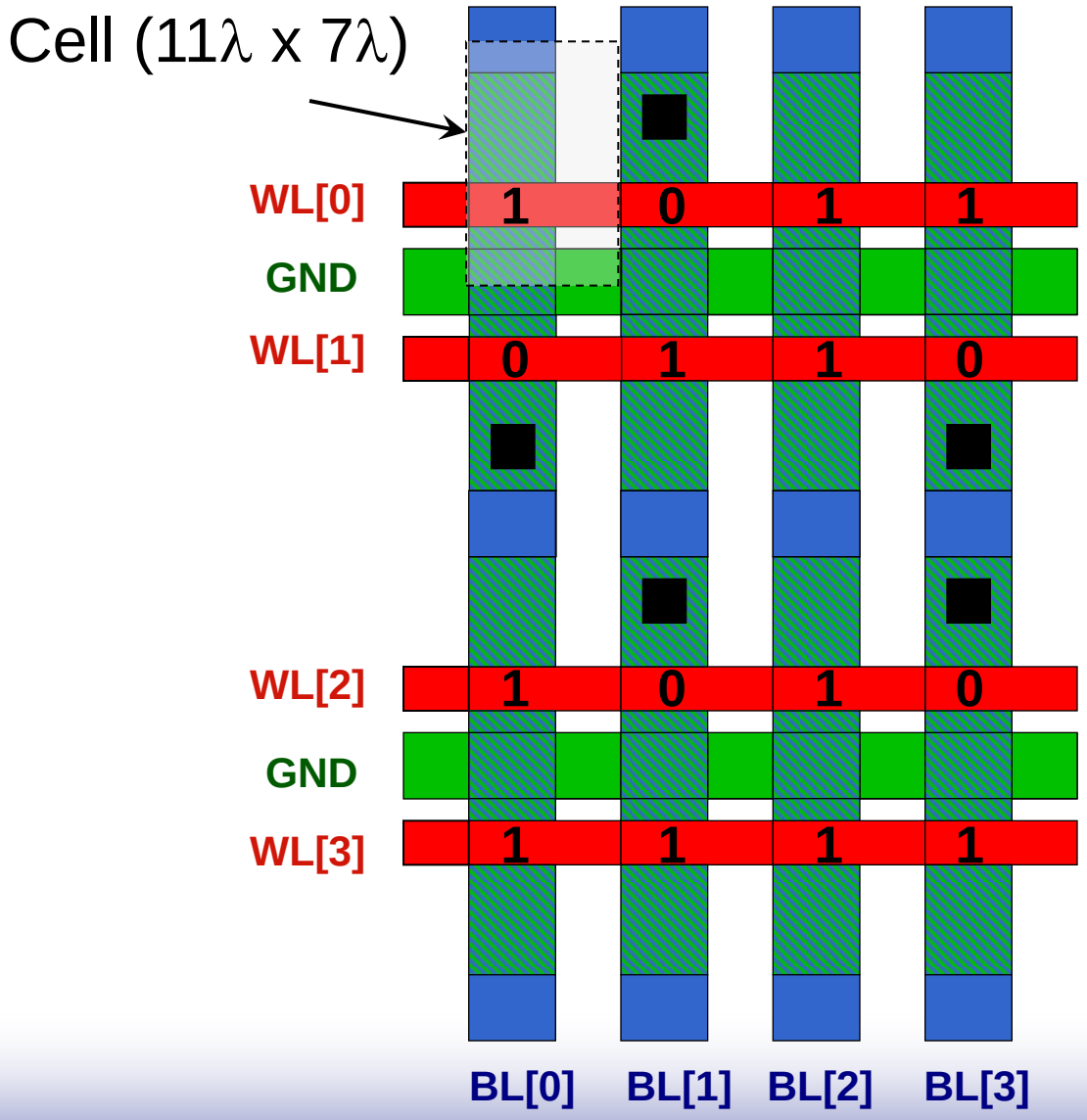
Polysilicon

Metal1

Diffusion

Metal1 on Diffusion

MOS NOR ROM Layout



Programming using the Contact Layer Only

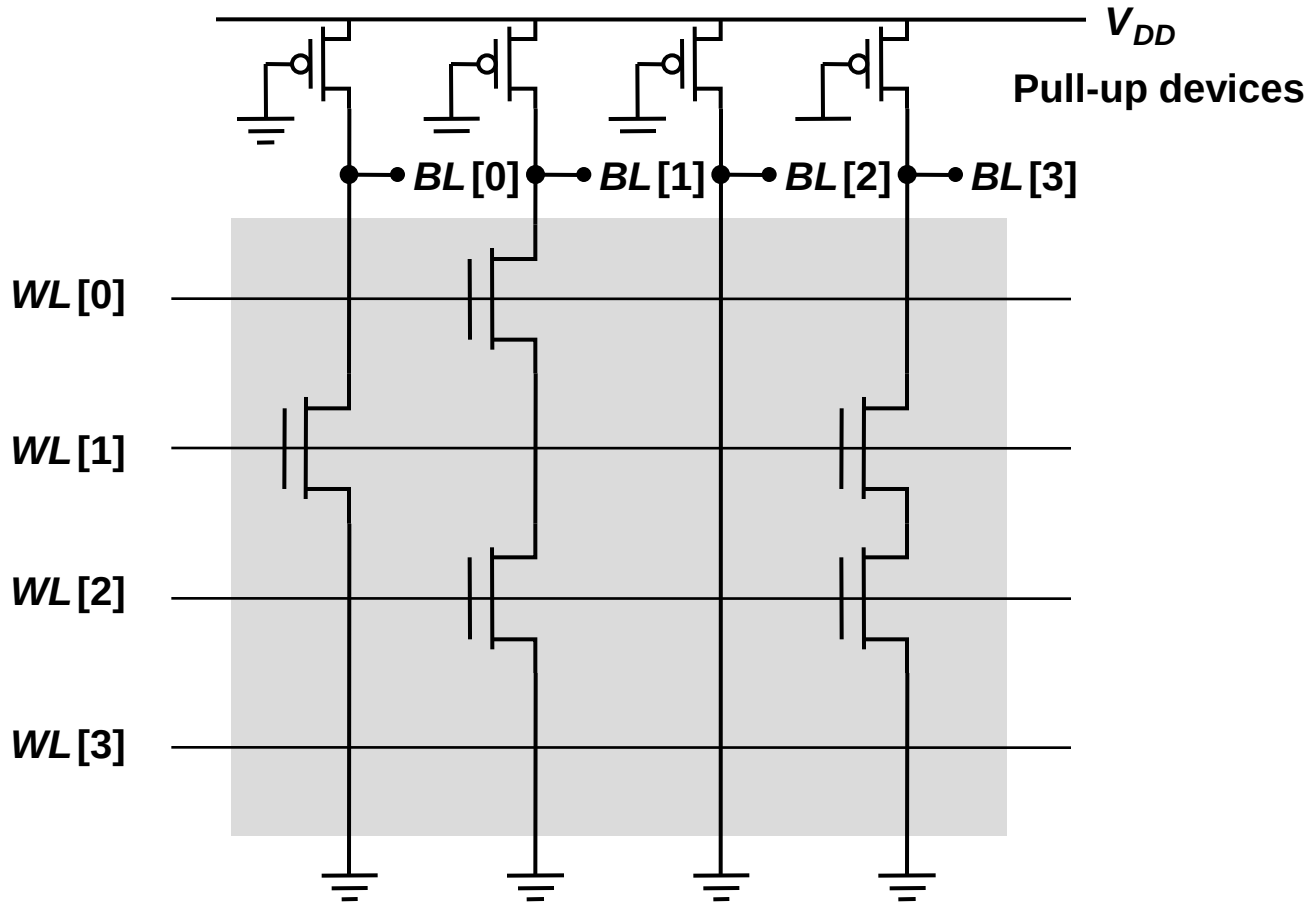
Polysilicon

Metal1

Diffusion

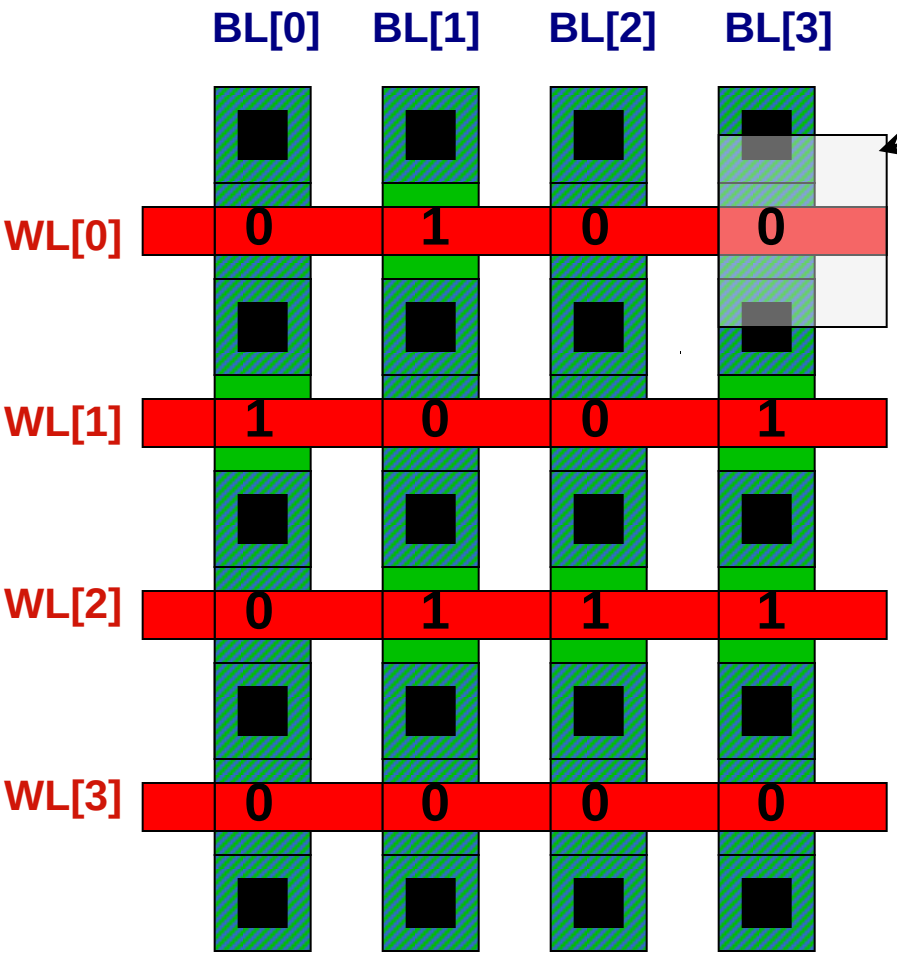
Metal1 on Diffusion

MOS NAND ROM



All word lines high by default with exception of selected row

MOS NAND ROM Layout



Cell (8λ x 7λ)

Programmming using the Metal-1 Layer Only

No contact to VDD or GND necessary; drastically reduced cell size

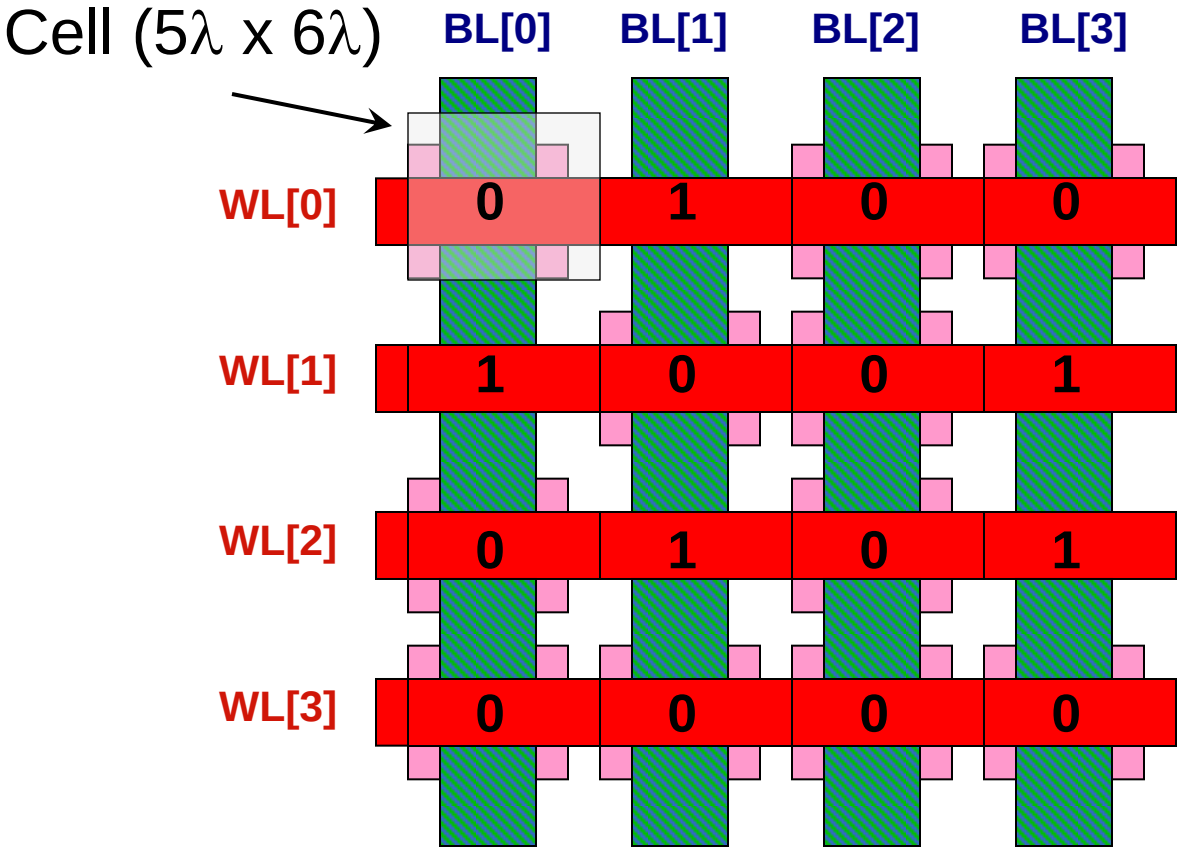
Loss in performance compared to NOR ROM

Polysilicon

Diffusion

Metal1 on Diffusion

NAND ROM Layout



Programmming using Implants Only

No contacts at all!

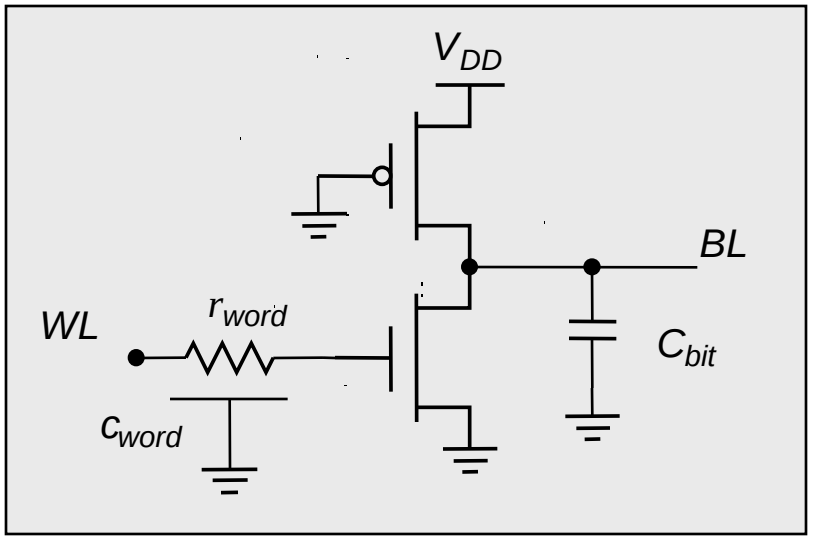
Polysilicon

Threshold-altering implant

Metal1 on Diffusion

Equivalent Transient Model for MOS NOR ROM

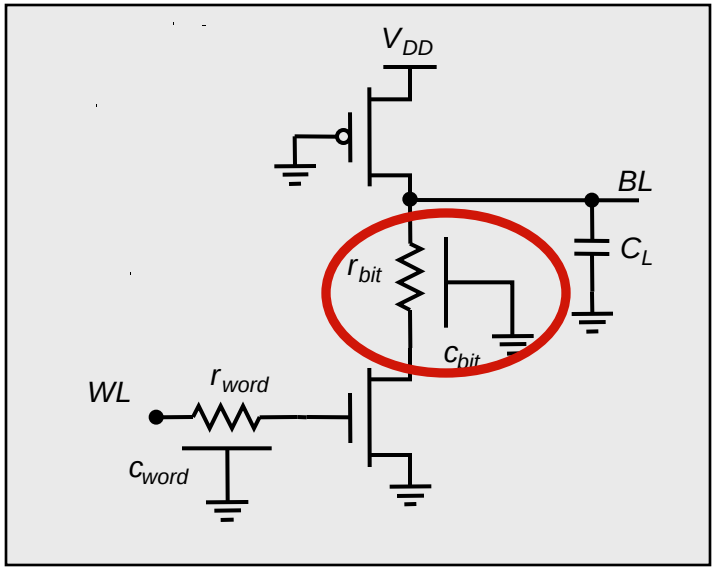
Model for NOR ROM



- Word line parasitics
  - Wire capacitance and gate capacitance
  - Wire resistance (polysilicon)
- Bit line parasitics
  - Resistance not dominant (metal)
  - Drain and Gate-Drain capacitance

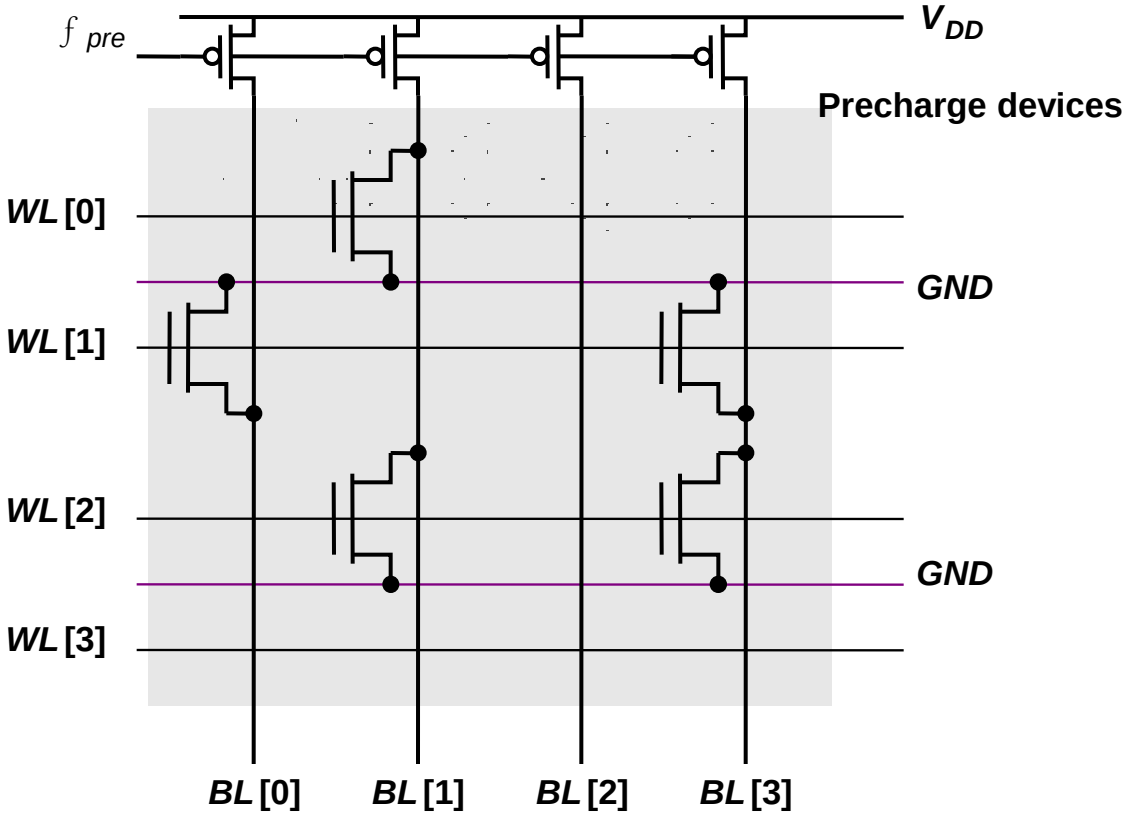
Equivalent Transient Model for MOS NAND ROM

Model for NAND ROM



- Word line parasitics
  - Similar to NOR ROM
- Bit line parasitics
  - Resistance of cascaded transistors dominates
  - Drain/Source and complete gate capacitance

Precharged MOS NOR ROM



PMOS precharge device can be made as large as necessary, but clock driver becomes harder to design.

ROM memories: user perspective

- Application specific ROMs
  - Designer can use any mask layer to program the device
- Commodity ROM chips
  - Mask programmable (one layer only)
    - Late processing phase: either contact or metal
  - Variant: only a **fraction** of die is mask programmable (compatible with SoC approach)

Conclusions

- Large variety of memory types according to:
  - Function
  - Volatility
  - Access pattern
  - I/O (ports)
  - Application

Conclusions

- Memory structure varies with size
  - Unidimensional array (of words)
  - Bidimensional array of words
    - Rows and colums
  - Tridimensional arrays of words
    - Rows, columns, and blocks

Conclusions

- ROM cores vary in
  - Structure (OR, NOR, NAND)
  - Programmable layers
    - Active area,
    - Contact
    - Threshold lowering implant
  - Pull-up mechanism
    - PMOS transistor load
    - PMOS precharging transistors

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