



**Universidade Federal de Santa Catarina**  
**Centro Tecnológico**  
Departamento de Informática e Estatística  
**Curso de Graduação em Ciências da Computação**



# **Sistemas Digitais**

**INE 5406**

## **Aula 4-P**

**Prototipagem com a placa de desenvolvimento DE2 da Altera.**

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**[www.inf.ufsc.br/~guntzel/ine5406/ine5406.html](http://www.inf.ufsc.br/~guntzel/ine5406/ine5406.html)**

# Prototipagem com Placa Altera DE2

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## ▶ Passos do projeto “Somador4bits”

### Organizando o Ambiente de Trabalho no Computador

1. Na pasta “Meus Documentos”, criar uma pasta com nome “Somador4bits”.
2. Acessar o sítio “[www.inf.ufsc.br/~guntzel/ine5406/aula4P](http://www.inf.ufsc.br/~guntzel/ine5406/aula4P)” e baixar os arquivos ali disponíveis para a pasta recém-criada. Os arquivos são:
  - > somador1bit.vhd
  - > somador4bits.vhd
  - > toplevel.vhd
  - > Setup\_Cyclone\_2C35\_DE2.tcl

# Prototipagem com Placa Altera DE2

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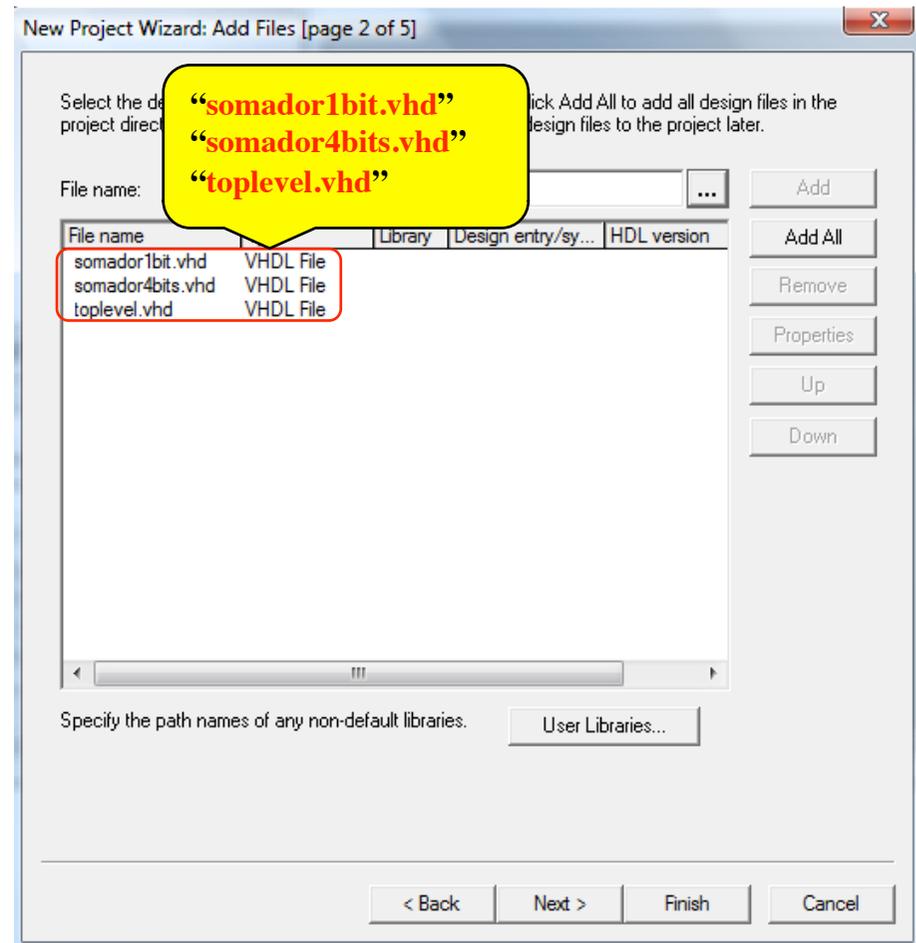
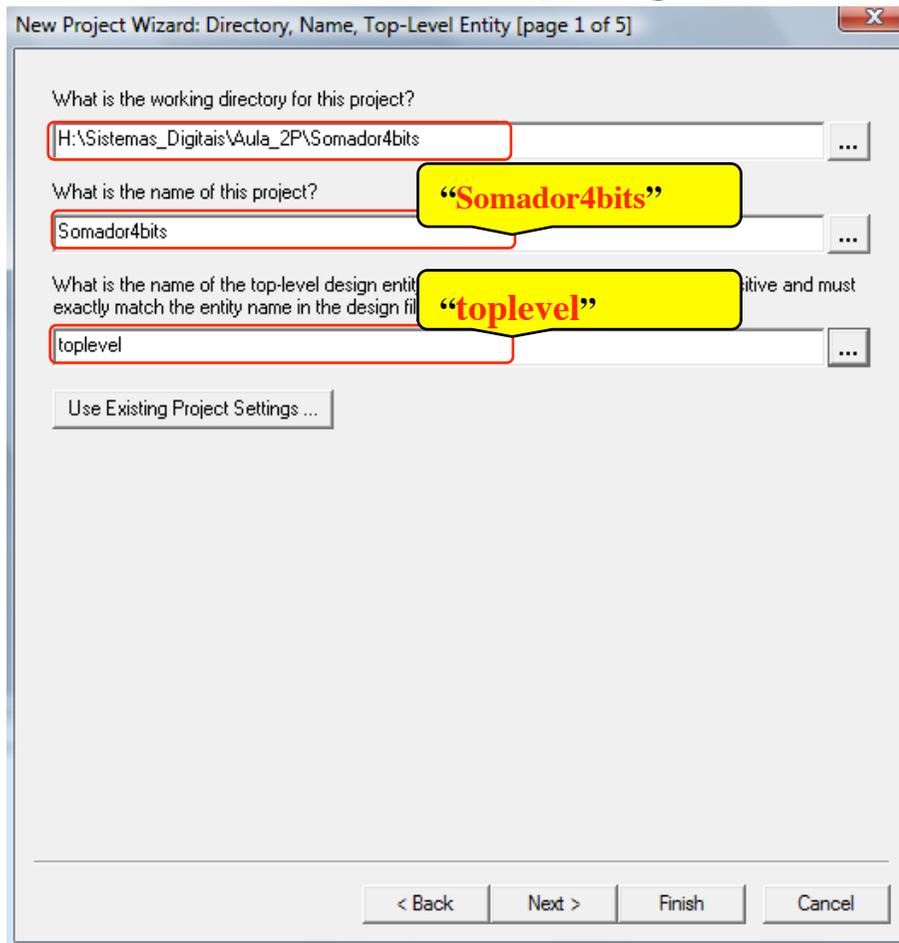
## ▶ Passos do projeto “somador4bits”

### Invocando o Quartus II e Criando um Projeto

3. Invocar o Quartus II (a partir do ícone na área de trabalho, ou a partir do “Iniciar->Programas” do windows, sub-menu “Altera”).
4. Na opção “New” (canto superior da janela), selecionar “New Project Wizard”.
5. Clicar em “Next”.
6. Selecionar o caminho para a pasta criada no passo 1 (clicando no botão identificado com “...”).
7. Na caixa de diálogo identificada por “What is the name of this project”, escrever “somador4bits”.
8. Na caixa de diálogo identificada por “What is the name of the toplevel design entity ...”, escrever “toplevel”. Clicar em “Next”.

# Prototipagem com Placa Altera DE2

## Passos do projeto “Somador4bits”



# Prototipagem com Placa Altera DE2

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## ▶ Passos do projeto “somador4bits” Invocando o Quartus II e Criando um Projeto (cont.)

9. Na caixa de diálogo identificada por “File Name:”, clicar na caixa com “...” e selecionar os três arquivos VHDL deste projeto (somador1bit.vhd, somador4bits.vhd e toplevel.vhd). Clicar em “Add All” e depois, clicar em “Next”.
10. Na caixa de diálogo “Device Family”, selecionar “Cyclone II”. Na lista identificada por “Available Devices”, selecionar EP2C35F672C6. Clicar em “Next”. (Ver próximo slide.)
11. Na caixa de diálogo “Simulation”, selecionar “ModelSim-Altera”. Clicar em Next.
12. Clicar em “Finish”. (Ver próximo slide.)

# Prototipagem com Placa Altera DE2

## Passos do projeto “Somador4bits”

New Project Wizard: Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Device family:  
Family: Cyclone II  
Devices: All

Target device:  
 Auto device selected by the Fitter  
 Specific device selected in 'Available devices' list

Show in 'Available device' list:  
Package: Any  
Pin count: Any  
Speed grade: Any  
 Show advanced devices  
 HardCopy compatible only

Available devices:

Name	Core v...	LEs	User I/...	Memor...	Embed...	PLL
EP2C20F484C8	1.2V	18752	315	239616	52	4
EP2C20F484I8	1.2V	18752	315	239616	52	4
EP2C20Q240C8	1.2V	18752	142	239616	52	4
EP2C35F484C6	1.2V	33216	322	483840	70	4
EP2C35F484C7	1.2V	33216	322	483840	70	4
EP2C35F484C8	1.2V	33216	322	483840	70	4
EP2C35F484I8	1.2V	33216	322	483840	70	4
EP2C35F672D6	1.2V	33216	475	483840	70	4

Companion device:  
HardCopy:   
 Limit DSP & RAM to HardCopy device resources

New Project Wizard: EDA Tool Settings [page 4 of 5]

Specify the other EDA tools -- in addition to the Quartus II software -- used with the project.

Design Entry/Synthesis:  
Tool name: <None>  
Format:   
 Run this tool automatically to synthesize the current design

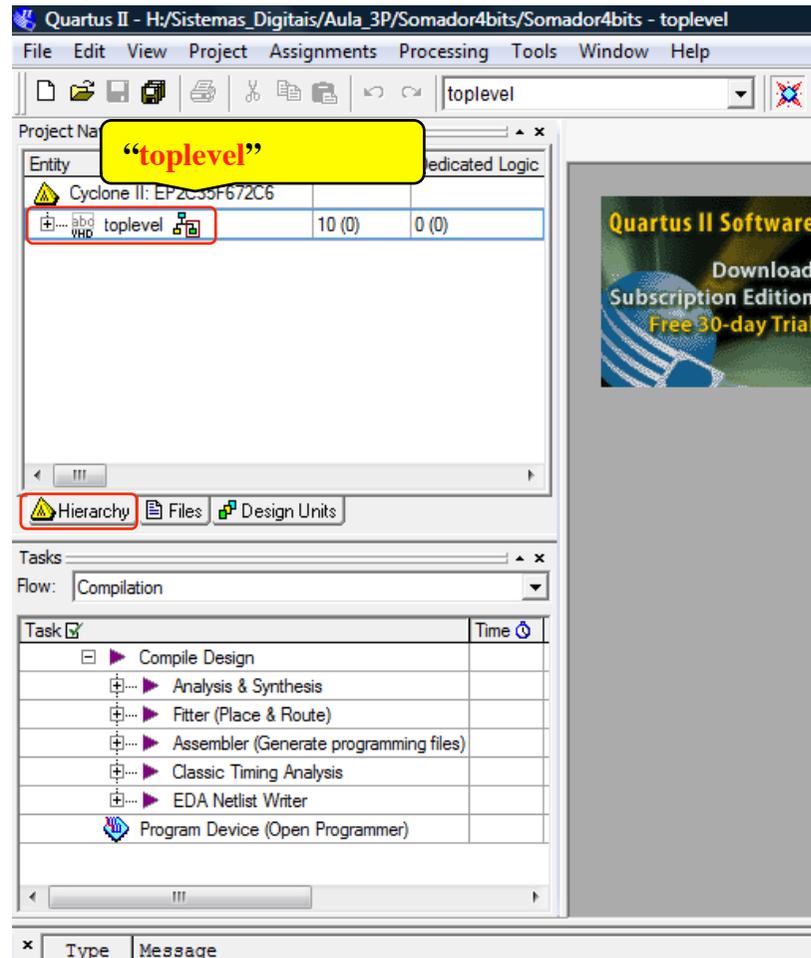
Simulation:  
Tool name: ModelSim-Altera  
Format: VHDL  
 Run gate-level simulation automatically after compilation

Timing Analysis:  
Tool name: <None>  
Format:   
 Run this tool automatically after compilation

# Prototipagem com Placa Altera DE2

## ▶ Passos do projeto “Somador4bits”

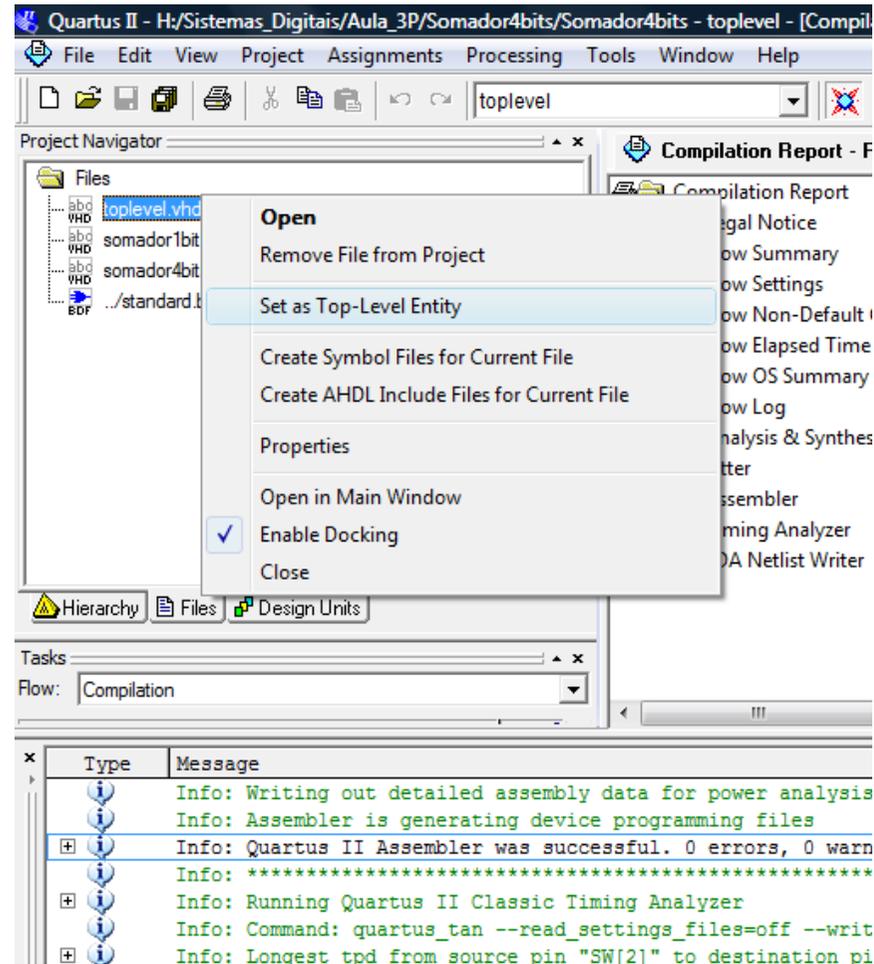
Verificar se o arquivo “toplevel.vdh” está setado como toplevel da hierarquia do projeto. Caso negativo, ajustar isso, conforme descrito no próximo slide.



# Prototipagem com Placa Altera DE2

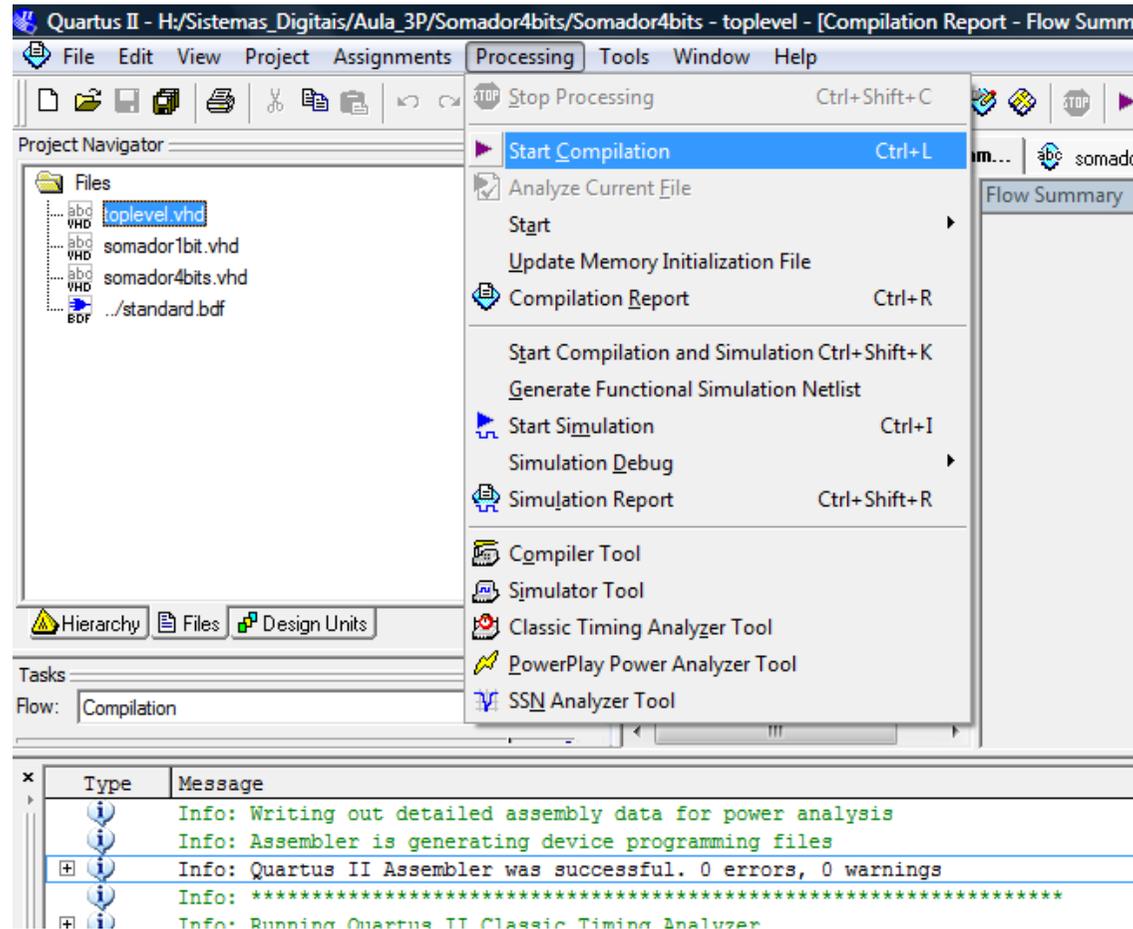
## ▶ Passos do projeto “Somador4bits”

Setando “toplevel.vdh”  
como toplevel da  
hierarquia do projeto.



# Prototipagem com Placa Altera DE2

## ▶ Compilar o projeto



# Prototipagem com Placa Altera DE2

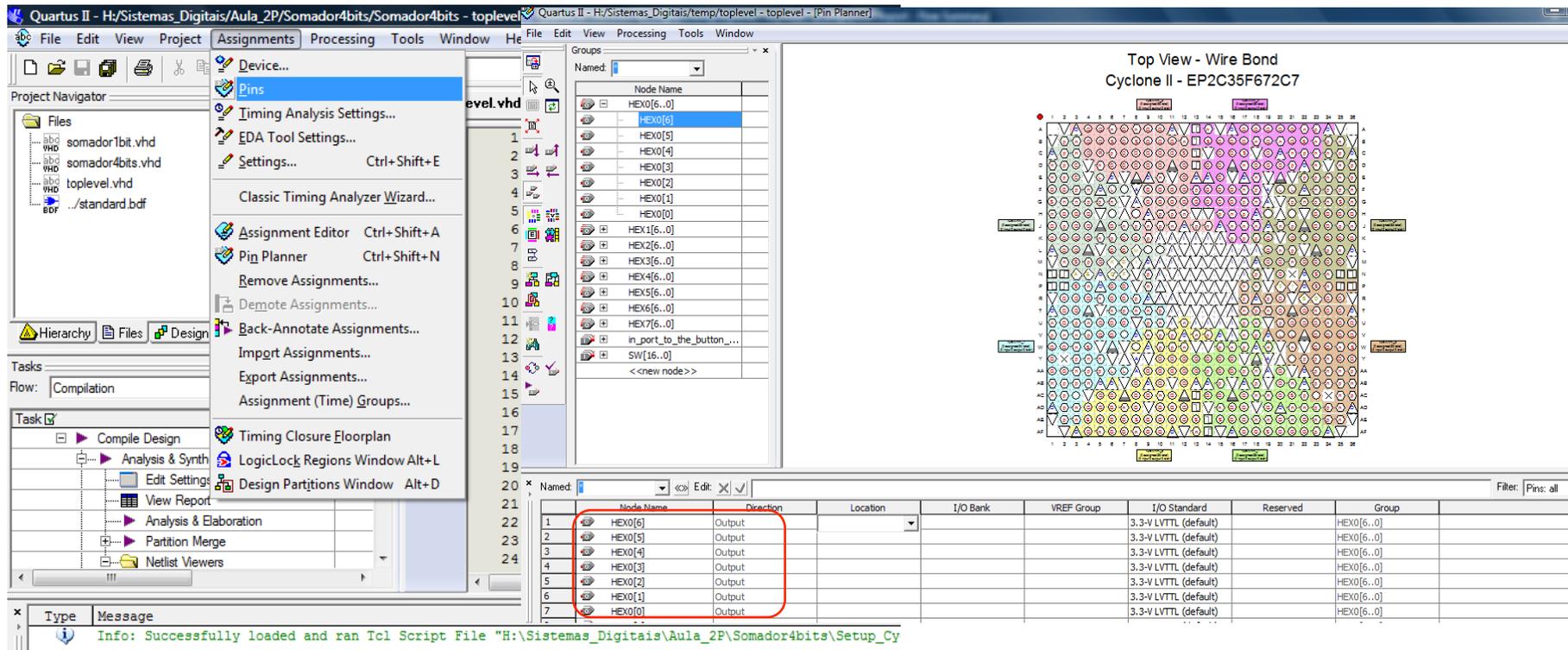
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## ▶ Passos do projeto “Somador4bits”

1. Anotar os seguintes dados mostrados na janela “Compilation Report – Flow Summary”:
  - Total combinational functions:
  - Dedicated logic elements:
2. Anotar os seguintes dados mostrados na janela “Message” (procurar pela linha que inicia por “Longest tpd from ...”):
  - tpd:
  - Source pin
  - Destination pin:

# Prototipagem com Placa Altera DE2

## ▶ Verificar o mapeamento dos pinos do FPGA



The screenshot shows the Quartus II Pin Planner interface. The 'Pins' menu is open, and the 'Top View - Wire Bond' window displays the Cyclone II EP2C35F672C7 pinout grid. A table at the bottom lists the pin assignments for the HEX0[6..0] outputs.

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Group
HEX0[6]	Output			3.3-V LVTTTL (default)			HEX0[6..0]
HEX0[5]	Output			3.3-V LVTTTL (default)			HEX0[6..0]
HEX0[4]	Output			3.3-V LVTTTL (default)			HEX0[6..0]
HEX0[3]	Output			3.3-V LVTTTL (default)			HEX0[6..0]
HEX0[2]	Output			3.3-V LVTTTL (default)			HEX0[6..0]
HEX0[1]	Output			3.3-V LVTTTL (default)			HEX0[6..0]
HEX0[0]	Output			3.3-V LVTTTL (default)			HEX0[6..0]

# Prototipagem com Placa Altera DE2

## ▶ Verificar o mapeamento dos pinos do FPGA

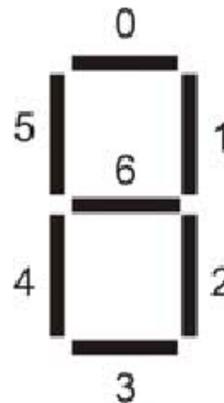
Mapeamentos do switches

Abrir o “DE2 UserManual.pdf”

Mapeamentos dos displays de 7 segmentos

Signal Name	FPGA Pin No.	Description
SW[0]	PIN_N25	Toggle Switch[0]
SW[1]	PIN_N26	Toggle Switch[1]
SW[2]	PIN_P25	Toggle Switch[2]
SW[3]	PIN_AE14	Toggle Switch[3]
SW[4]	PIN_AF14	Toggle Switch[4]
SW[5]	PIN_AD13	Toggle Switch[5]
SW[6]	PIN_AC13	Toggle Switch[6]
SW[7]	PIN_C13	Toggle Switch[7]
SW[8]	PIN_B13	Toggle Switch[8]
SW[9]	PIN_A13	Toggle Switch[9]
SW[10]	PIN_N1	Toggle Switch[10]
SW[11]	PIN_P1	Toggle Switch[11]
SW[12]	PIN_P2	Toggle Switch[12]
SW[13]	PIN_T7	Toggle Switch[13]
SW[14]	PIN_U3	Toggle Switch[14]
SW[15]	PIN_U4	Toggle Switch[15]
SW[16]	PIN_V1	Toggle Switch[16]
SW[17]	PIN_V2	Toggle Switch[17]

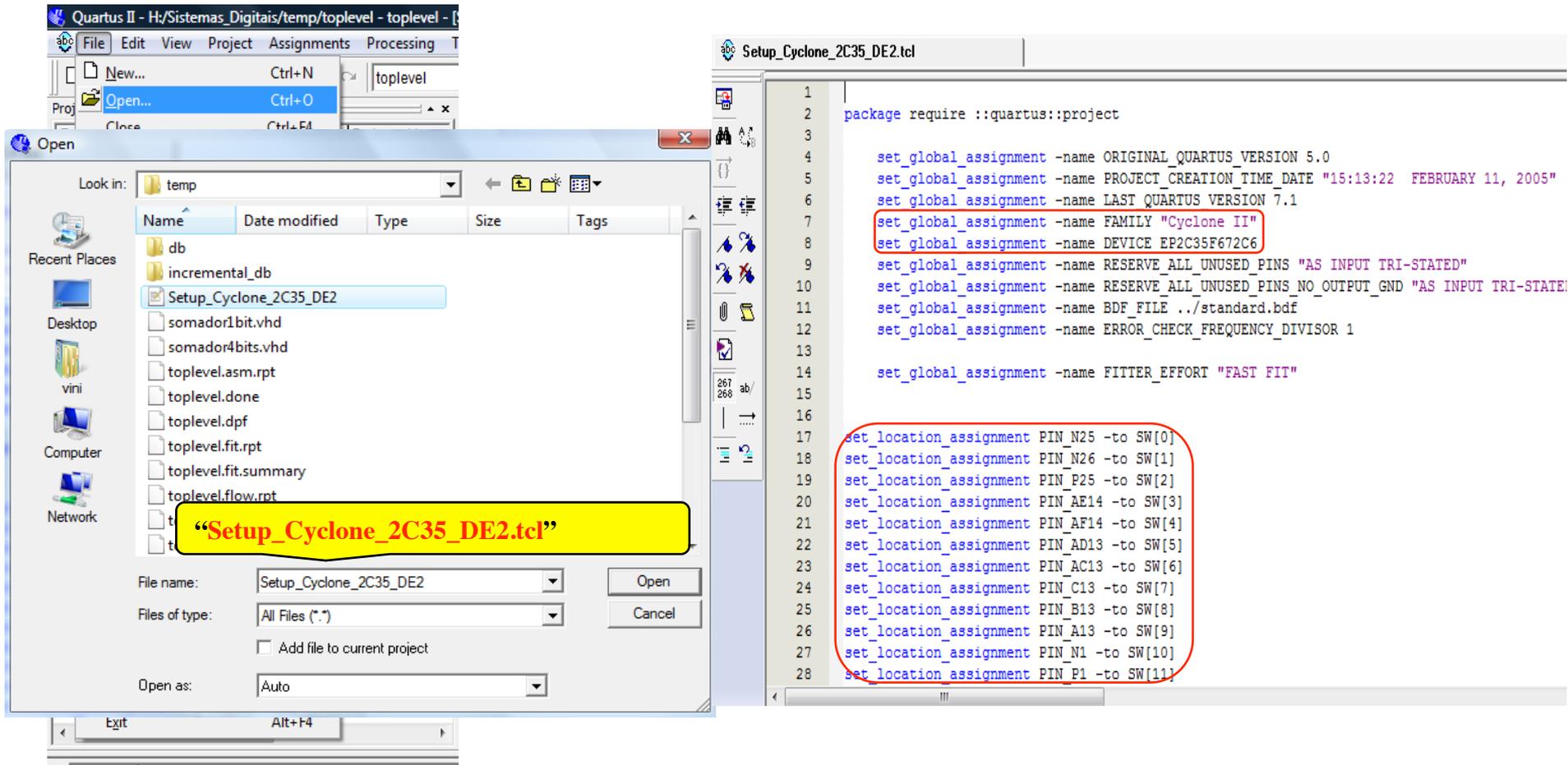
Posição e index de cada segmento do display de 7 segmentos



Signal Name	FPGA Pin No.	Description
HEX0[0]	PIN_AF10	Seven Segment Digit 0[0]
HEX0[1]	PIN_AB12	Seven Segment Digit 0[1]
HEX0[2]	PIN_AC12	Seven Segment Digit 0[2]
HEX0[3]	PIN_AD11	Seven Segment Digit 0[3]
HEX0[4]	PIN_AE11	Seven Segment Digit 0[4]
HEX0[5]	PIN_V14	Seven Segment Digit 0[5]
HEX0[6]	PIN_V13	Seven Segment Digit 0[6]
HEX1[0]	PIN_V20	Seven Segment Digit 1[0]
HEX1[1]	PIN_V21	Seven Segment Digit 1[1]
HEX1[2]	PIN_W21	Seven Segment Digit 1[2]
HEX1[3]	PIN_Y22	Seven Segment Digit 1[3]
HEX1[4]	PIN_AA24	Seven Segment Digit 1[4]
HEX1[5]	PIN_AA23	Seven Segment Digit 1[5]
HEX1[6]	PIN_AB24	Seven Segment Digit 1[6]
HEX2[0]	PIN_AB23	Seven Segment Digit 2[0]
HEX2[1]	PIN_V22	Seven Segment Digit 2[1]

# Prototipagem com Placa Altera DE2

## ▶ O script “Setup\_Cyclone\_2C35\_DE2.tcl”

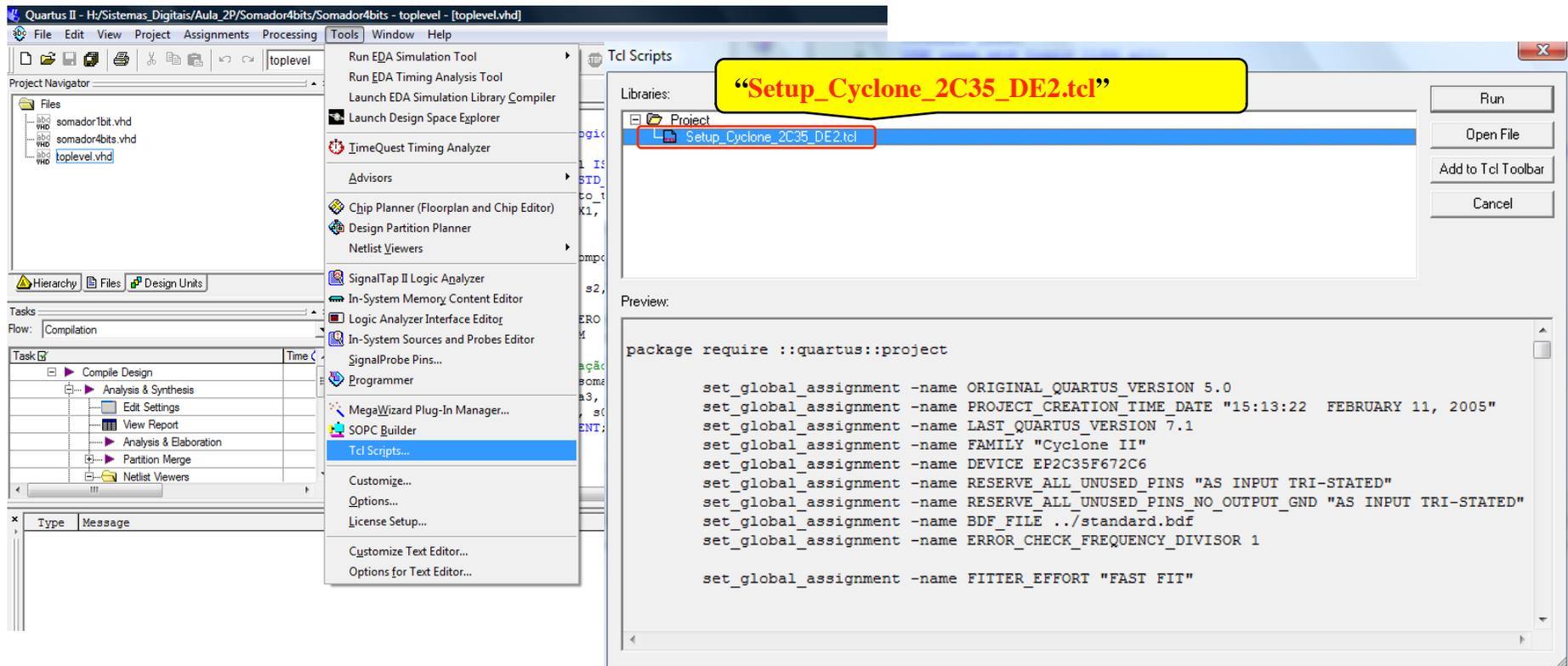


The image shows a screenshot of the Quartus II software interface. On the left, an 'Open' dialog box is displayed, showing the file 'Setup\_Cyclone\_2C35\_DE2.tcl' selected in the 'temp' directory. The file name is highlighted in a yellow box. On the right, the 'Setup\_Cyclone\_2C35\_DE2.tcl' script is open in an editor. The script contains the following TCL commands:

```
1 package require ::quartus::project
2
3
4 set_global_assignment -name ORIGINAL_QUARTUS_VERSION 5.0
5 set_global_assignment -name PROJECT_CREATION_TIME_DATE "15:13:22 FEBRUARY 11, 2005"
6 set_global_assignment -name LAST_QUARTUS_VERSION 7.1
7 set_global_assignment -name FAMILY "Cyclone II"
8 set_global_assignment -name DEVICE EP2C35F672C6
9
10 set_global_assignment -name RESERVE_ALL_UNUSED_PINS "AS INPUT TRI-STATE"
11 set_global_assignment -name RESERVE_ALL_UNUSED_PINS_NO_OUTPUT_GND "AS INPUT TRI-STATE"
12 set_global_assignment -name BDF_FILE ../standard.bdf
13 set_global_assignment -name ERROR_CHECK_FREQUENCY_DIVISOR 1
14
15
16
17 set_location_assignment PIN_N25 -to SW[0]
18 set_location_assignment PIN_N26 -to SW[1]
19 set_location_assignment PIN_P25 -to SW[2]
20 set_location_assignment PIN_AE14 -to SW[3]
21 set_location_assignment PIN_AF14 -to SW[4]
22 set_location_assignment PIN_AD13 -to SW[5]
23 set_location_assignment PIN_AC13 -to SW[6]
24 set_location_assignment PIN_C13 -to SW[7]
25 set_location_assignment PIN_B13 -to SW[8]
26 set_location_assignment PIN_A13 -to SW[9]
27 set_location_assignment PIN_N1 -to SW[10]
28 set_location_assignment PIN_P1 -to SW[11]
```

# Prototipagem com Placa Altera DE2

## ▶ Executar script de mapeamento dos pinos



The screenshot shows the Quartus II interface with the 'Tools' menu open and 'Tcl Scripts...' selected. A 'Tcl Scripts' dialog box is open, displaying a list of scripts under the 'Project' library. The script 'Setup\_Cyclone\_2C35\_DE2.tcl' is highlighted. A yellow callout box points to this script with the text "Setup\_Cyclone\_2C35\_DE2.tcl". The 'Preview' section of the dialog shows the following Tcl code:

```
package require ::quartus::project

set_global_assignment -name ORIGINAL_QUARTUS_VERSION 5.0
set_global_assignment -name PROJECT_CREATION_TIME_DATE "15:13:22 FEBRUARY 11, 2005"
set_global_assignment -name LAST_QUARTUS_VERSION 7.1
set_global_assignment -name FAMILY "Cyclone II"
set_global_assignment -name DEVICE EP2C35F672C6
set_global_assignment -name RESERVE_ALL_UNUSED_PINS "AS INPUT TRI-STATED"
set_global_assignment -name RESERVE_ALL_UNUSED_PINS_NO_OUTPUT_GND "AS INPUT TRI-STATED"
set_global_assignment -name BDF_FILE ../standard.bdf
set_global_assignment -name ERROR_CHECK_FREQUENCY_DIVISOR 1

set_global_assignment -name FITTER_EFFORT "FAST FIT"
```

# Prototipagem com Placa Altera DE2

## ▶ Verificar o mapeamento dos pinos do FPGA

The screenshot shows the Quartus II Pin Planner interface. The top view of the Cyclone II EP2C35F672C6 is displayed, showing the pin locations and their assignments. A table below the top view lists the pin assignments for nodes SW[0] through SW[6].

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Group
SW[0]	Unknown	PIN_N25	5	B5_N1	3.3-V LVTTTL (default)		
SW[1]	Unknown	PIN_N26	5	B5_N1	3.3-V LVTTTL (default)		
SW[2]	Unknown	PIN_P25	6	B6_N0	3.3-V LVTTTL (default)		
SW[3]	Unknown	PIN_AE14	7	B7_N1	3.3-V LVTTTL (default)		
SW[4]	Unknown	PIN_AF14	7	B7_N1	3.3-V LVTTTL (default)		
SW[5]	Unknown	PIN_AD13	8	B8_N0	3.3-V LVTTTL (default)		
SW[6]	Unknown	PIN_AC13	8	B8_N0	3.3-V LVTTTL (default)		

# Prototipagem com Placa Altera DE2

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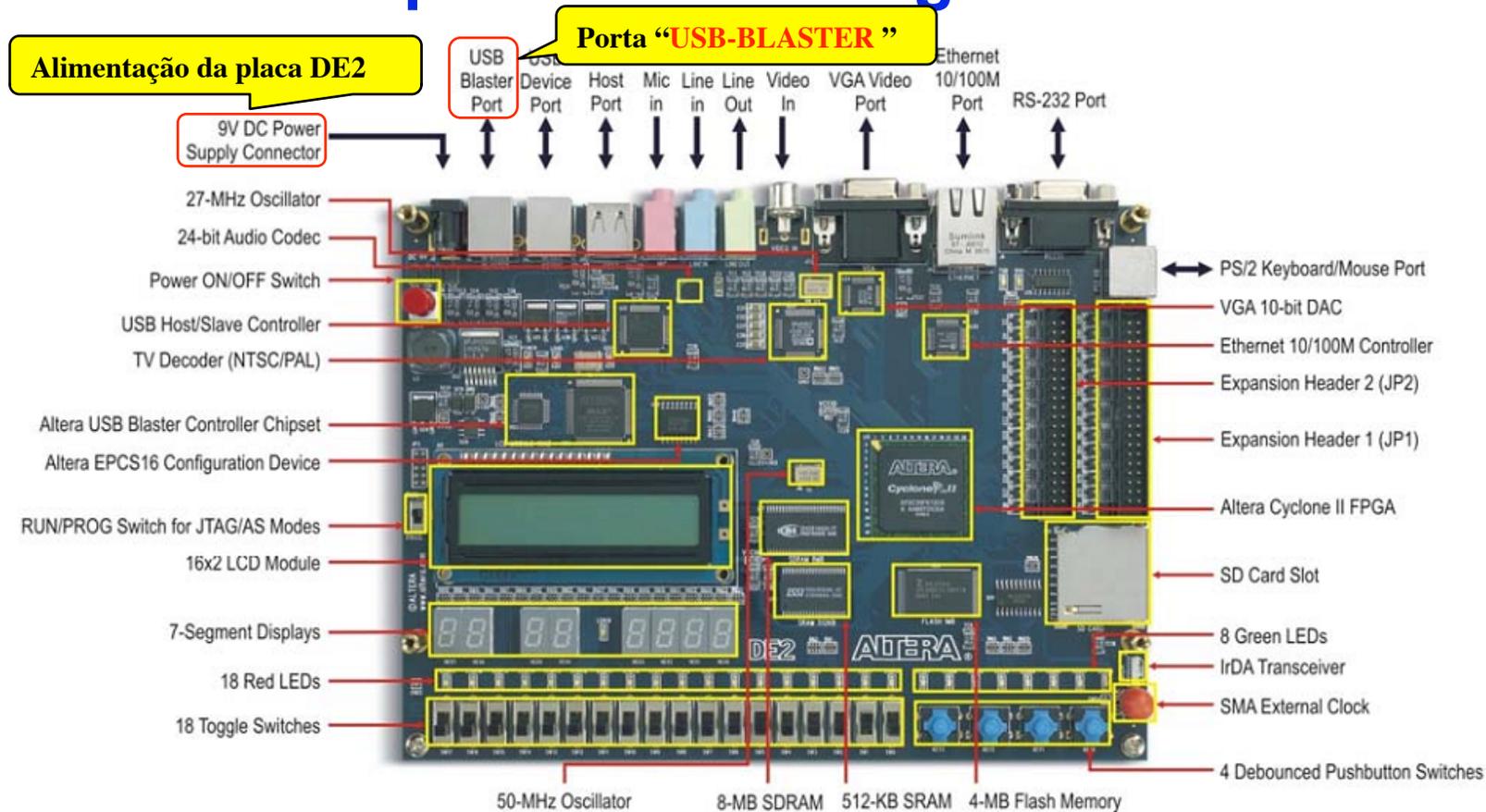
## ▶ Passos do projeto “Somador4bits”

### Compilar

1. Processing -> Start Compilation
2. Aguardar mensagem “Quartus II Full Compilation Succesfull” (ou mensagem de erro)

# Prototipagem com Placa Altera DE2

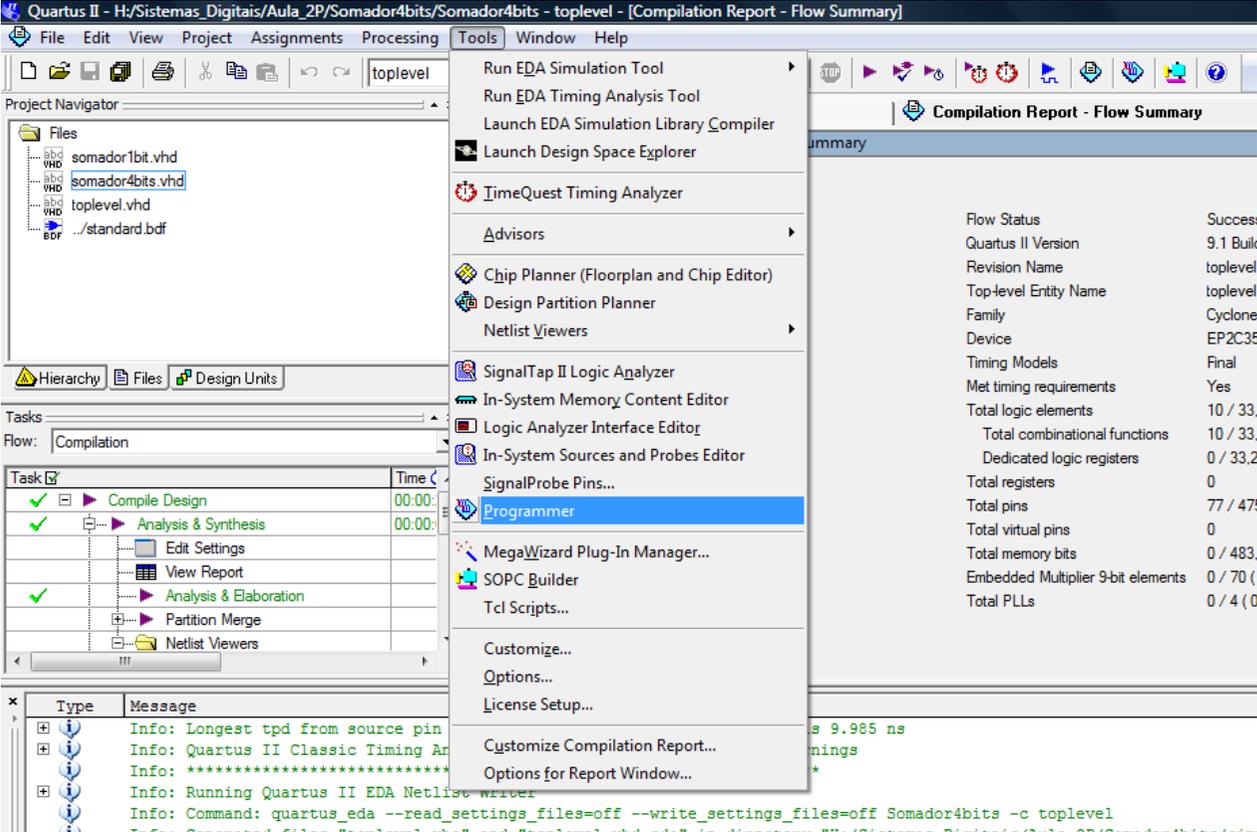
## ▶ Conectar a placa no PC e ligá-la



Ler manual da placa DE2. (Baixar de “<http://www.inf.ufsc.br/~guntzel/ine5406/DE2/>” )

# Prototipagem com Placa Altera DE2

## ▶ Baixar o projeto para a placa



The screenshot displays the Quartus II IDE interface during a compilation process. The main window shows the 'Compilation Report - Flow Summary' for the project 'Somador4bits'. The 'Tools' menu is open, with the 'Programmer' option highlighted. The 'Tasks' pane on the left shows the compilation flow, including 'Compile Design', 'Analysis & Synthesis', and 'Analysis & Elaboration'. The 'Messages' pane at the bottom shows the command used to run the compilation: `quartus_eda --read_settings_files=off --write_settings_files=off Somador4bits -c toplevel`.

Flow Status	Success
Quartus II Version	9.1 Build
Revision Name	toplevel
Top-level Entity Name	toplevel
Family	Cyclone
Device	EP2K35
Timing Models	Final
Met timing requirements	Yes
Total logic elements	10 / 33,2
Total combinational functions	10 / 33,2
Dedicated logic registers	0 / 33,2
Total registers	0
Total pins	77 / 475
Total virtual pins	0
Total memory bits	0 / 483,2
Embedded Multiplier 9-bit elements	0 / 70 (0)
Total PLLs	0 / 4 (0)

# Prototipagem com Placa Altera DE2

## ▶ Baixar o projeto para a placa

